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MS-7399

Version 4.0

CPU:

Intel Prescott (L2=2MB)
 Intel Cendar Mill (65nm)
 Intel Smithfield (90nm Dual core)
 Intel Presler (65nm Dual core)
 Intel Conroe (65nm Dual core)
 Intel Kentsfield
 Intel Yorkfield
 Intel Wolfdale

System Chipset:

nVidia - MCP73PV

On Board Chipset:

BIOS -- SPI FLASH 4Mb
 Azalia CODEC(ALC 888S)
 LPC Super I/O -- ITE8718F
 LAN-Realtek RTL8211BL

Main Memory:

DDR II * 2 (Max 2GB)

Expansion Slots:

PCI Express X16 SLOT * 1
 PCI Express X1 SLOT * 1
 PCI 2.3 SLOT * 2

Intersil PWM:

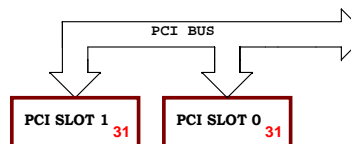
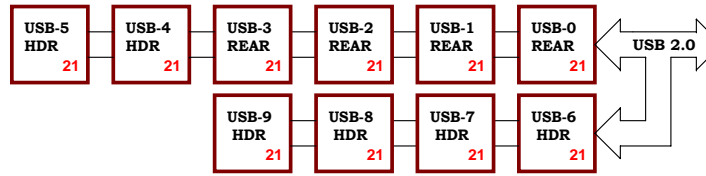
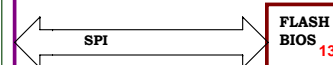
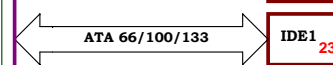
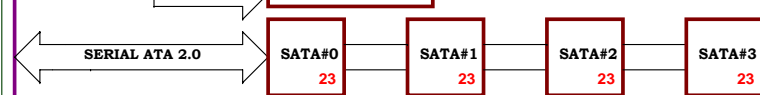
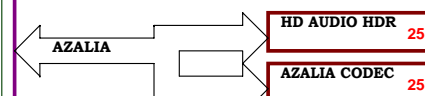
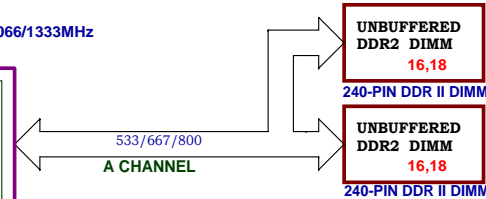
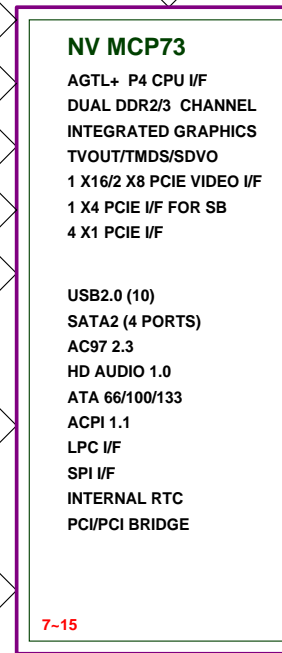
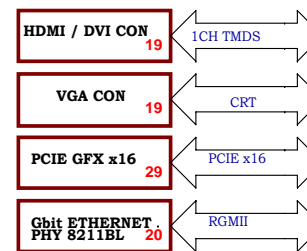
Controller: Intersil 6312 3 Phase

Block Diagram

LGA775 CONROE
LGA775 SMITHFIELD
LGA775 PENTIUM D, EE
LGA775 PRESCOTT 4,5,6

4X DATA
2X ADDRESS

AGTL+
533/800/1066/1333MHz



CPU CORE POWER 29

CPU VTT POWER
MCP73 CORE POWER
PCIE & SB POWER 27,28

DDR2 DRAM POWER 28

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ITE LPC SIO 8718F 22



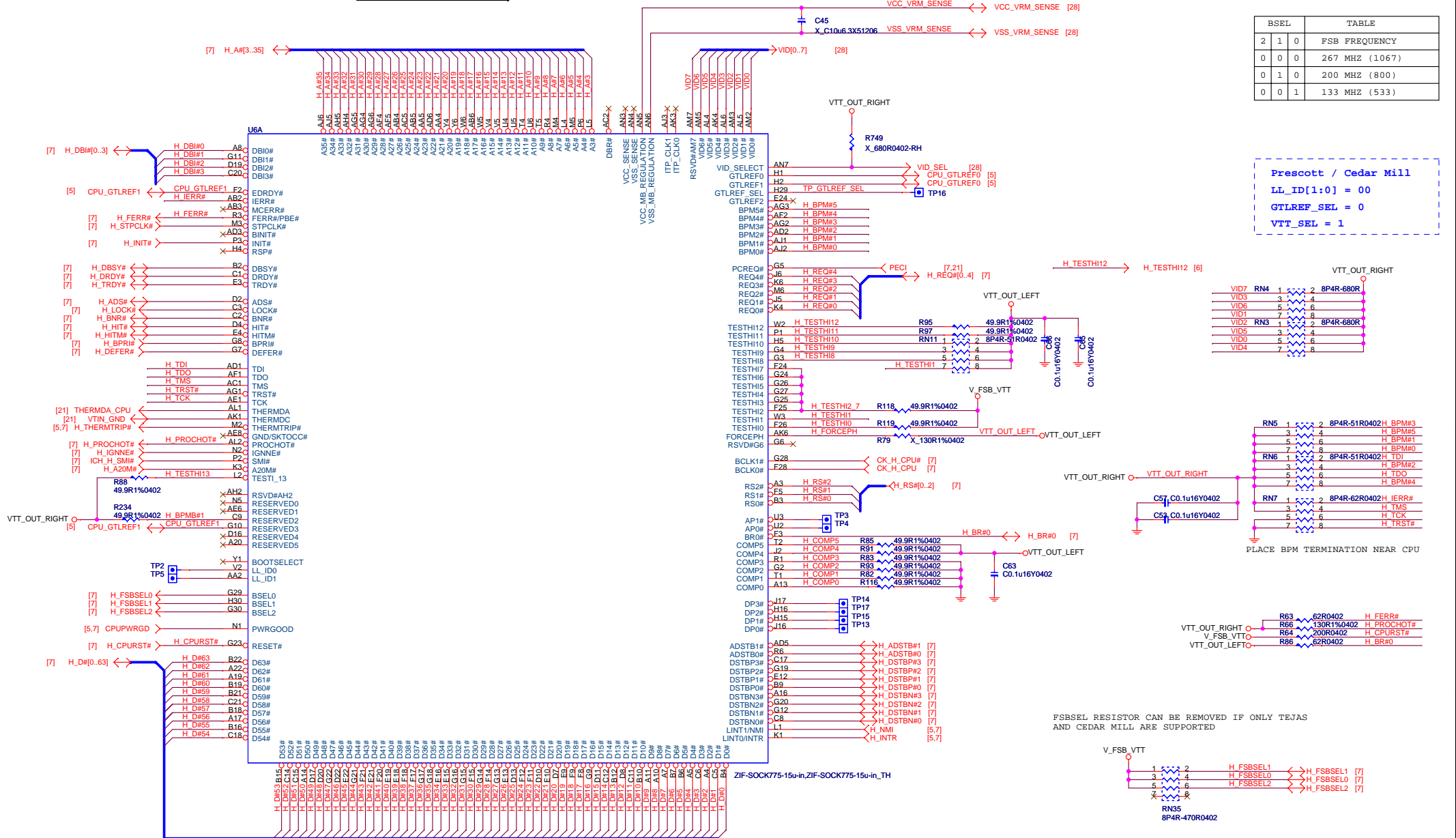
MCP73 GPIO Config.

GPIO Pin	Type	Primary State
GPIO_2/NMI/PS2_CLK0	I/O(S5_3.3V)	TMDS_DET1
GPIO_3/SMI#/PS2_DATA0	I/O(S5_3.3V)	TMDS_DET2
GPIO_4/SCI/INTR/PS2_CLK1	I/O(S5_3.3V)	Unused
GPIO_5/INIT#/PS2_DATA1	I/O(S5_3.3V)	OBR1
GPIO_6/FERR#/SYS_SERR#/IGPU_GPIO6	I/O(S5_3.3V)	Unused
GPIO_7/NFERR#/SYS_PERR#/IGPU_GPIO7	I/O(S5_3.3V)	Unused
GPIO_8/SPI_DI	I/O(S5_3.3V)	Unused
GPIO_9/SPI_DO	I/O(S5_3.3V)	Unused
GPIO_10/SPI_CS0	I/O(S5_3.3V)	Unused
GPIO_11/SPI_CLK	I/O(S5_3.3V)	Unused
LPC_DRQ1#/GPIO_19/FANRPM1	I/O(3.3V)	Unused
PROCHOT#/GPIO_20	I/O(CPU_VTT)	H_PROCHOT#
PE_WAKE#/GPIO_21	I/O(S5_3.3V)	WAKE#
HDA_SDATA_IN0/GPIO_22	I/O(S5_3.3V)	HDA_SDATA_IN
HDA_SDATA_IN1/GPIO_23/MGPIO_0	I/O(S5_3.3V)	Unused
HDA_SDATA_IN2/GPIO_24/MGPIO_2	I/O(3.3V)	Unused
USB_OC0#/GPIO_25	I/O(S5_3.3V)	OC#1
USB_OC1#/GPIO_26	I/O(S5_3.3V)	OC#2
USB_OC2#/GPIO_27	I/O(S5_3.3V)	OC#3
USB_OC3#/GPIO_28	I/O(S5_3.3V)	Pull Hi
USB_OC4#/GPIO_29	I/O(S5_3.3V)	Pull Hi
PCI_PME#/GPIO_30	I/O(S5_3.3V)	PCI_PME#
SIO_PME#/GPIO_31	I/O(S5_3.3V)	SIO_PME#
EXT_SMI#/GPIO_32	I/O(S5_3.3V)	LPC_SMI#
SUS_CLK/GPIO_34	I/O(S5_3.3V)	Unused
MII0_INTR/GPIO_35	I/O(S5_3.3V)	RGMI0_INTR#
MII0_PXER/GPIO_36/PWR_LED#	I/O(S5_3.3V)	RGMI0_RX_ER
MII0_PWRDWN/GPIO_37	I/O(S5_3.3V)	RGMI0_PREDN
PCI_REQ3#/GPIO_38/RS232_CTS#	I/O(3.3V)	PREQ#3
PCI_GNT3#/GPIO_39/RS232_RTS#	I/O(3.3V)	Unused
PCI_REQ2#/GPIO_40/RS232_DSR#	I/O(3.3V)	PREQ#2
PCI_GNT2#/GPIO_41/RS232_DTR#	I/O(3.3V)	PGNT#2
LPC_RESET#/GPIO_42	I/O(3.3V)	Unused
PCI_PERR#/GPIO_43/RS232_DCD#	I/O(3.3V)	PERR#
HDA_SYNC/GPIO_44	I/O(3.3V)	AZ_SYNC_R
HDA_SDATA_OUT/GPIO_45	I/O(3.3V)	HDA_SDATA_OUT
LPC_DRQ0#/GPIO_50	I/O(3.3V)	LPC_DRQ#0
PCI_REQ4#/GPIO52/RS232_SIN#	I/O(3.3V)	PREQ#4
PCI_GNT4#/GPIO_53/RS232_SOUT#	I/O(3.3V)	Unused
A20GATE/GPIO_55	I/O(3.3V)	A20GATE
KBRDRSTIN#/GPIO_56	I/O(3.3V)	KBRST#
SATA_LED#/GPIO_57	A(3.3V)	SATALED#
THERMTRIP#/GPIO_58	I/O(CPU_VTT)	H_THERMTRIP#
THERM#/GPIO_59	I/O(3.3V)	Unused
FANRPM0/GPIO_60	I/O(3.3V)	OBR2
FANCTL0/GPIO_61	I/O(3.3V)	AUDIO_FRONT_IO
FANCTL1/GPIO_62	I/O(3.3V)	DEPOP_GPIO
CABLE_DET_P/GPIO_63	I/O(3.3V)	ATADETO

PCI Config.

DEVICE	MCP1 INTX Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTX# PCI_INTY# PCI_INTZ# PCI_INTW#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTY# PCI_INTZ# PCI_INTW# PCI_INTX#	PREQ#1 PGNT#1	AD22	PCICLK1
1394	PCI_INTW#	PREQ#2 PGNT#2	AD23	1394_PCLK

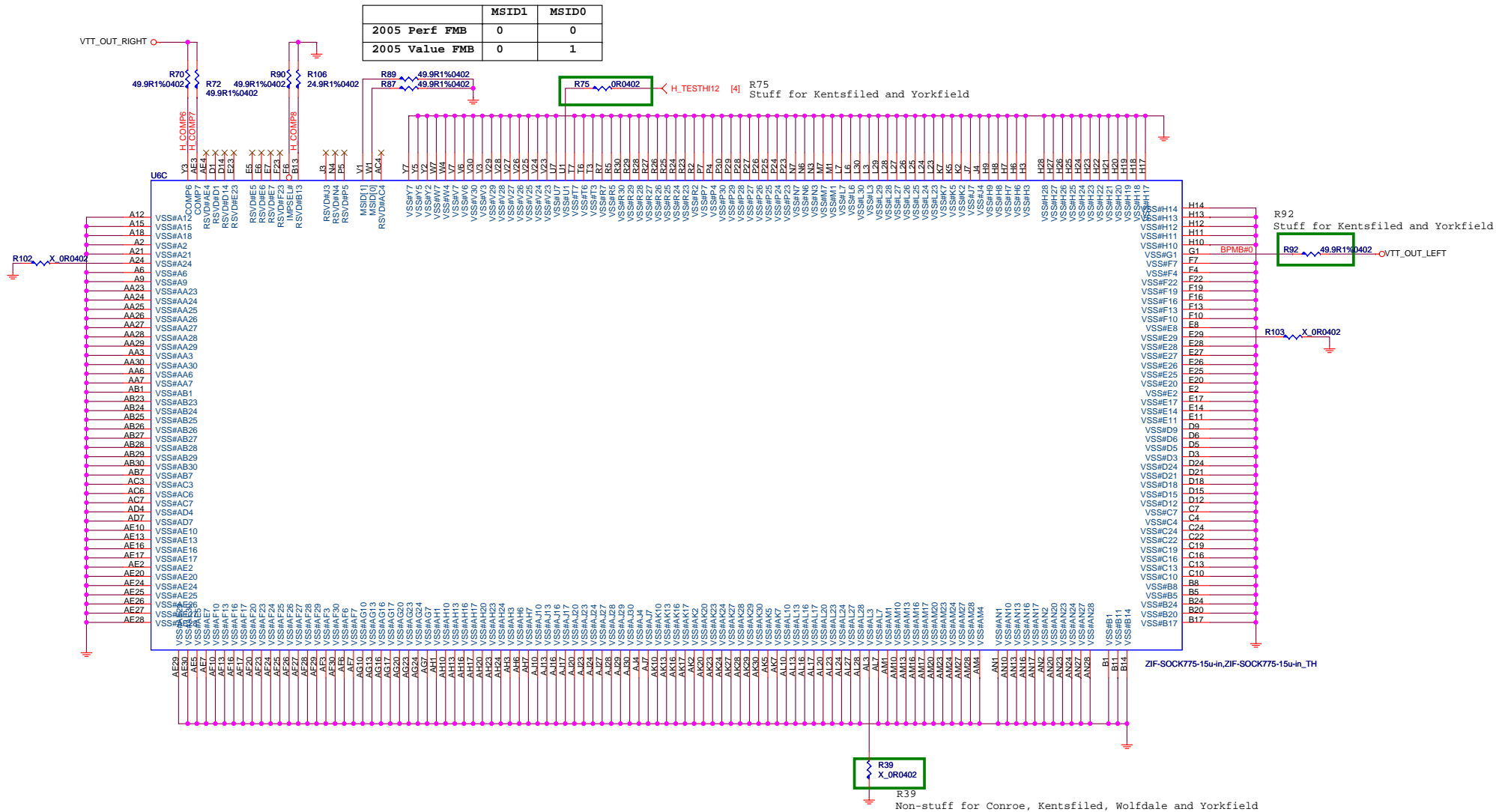
CPU SIGNAL BLOCK

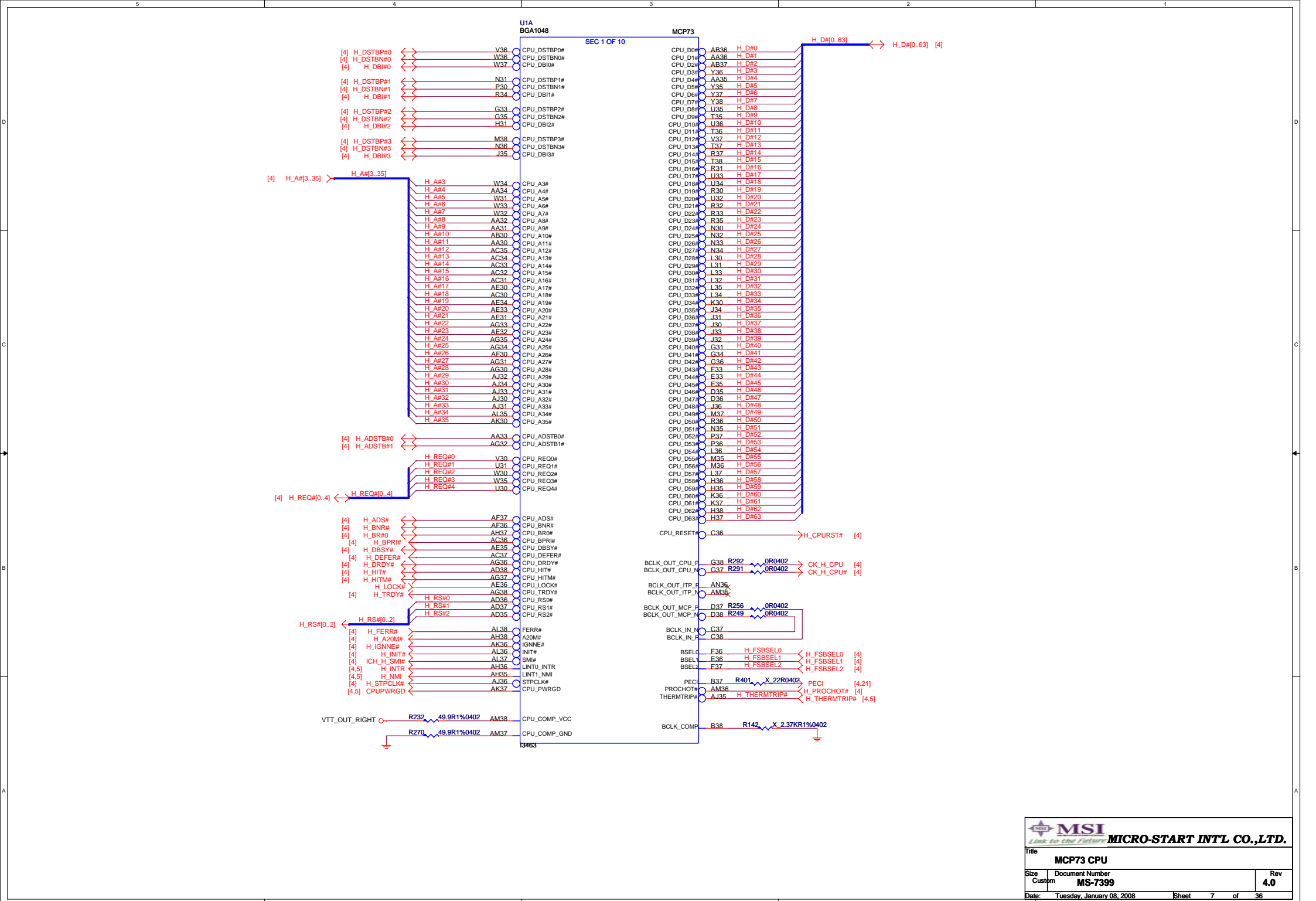


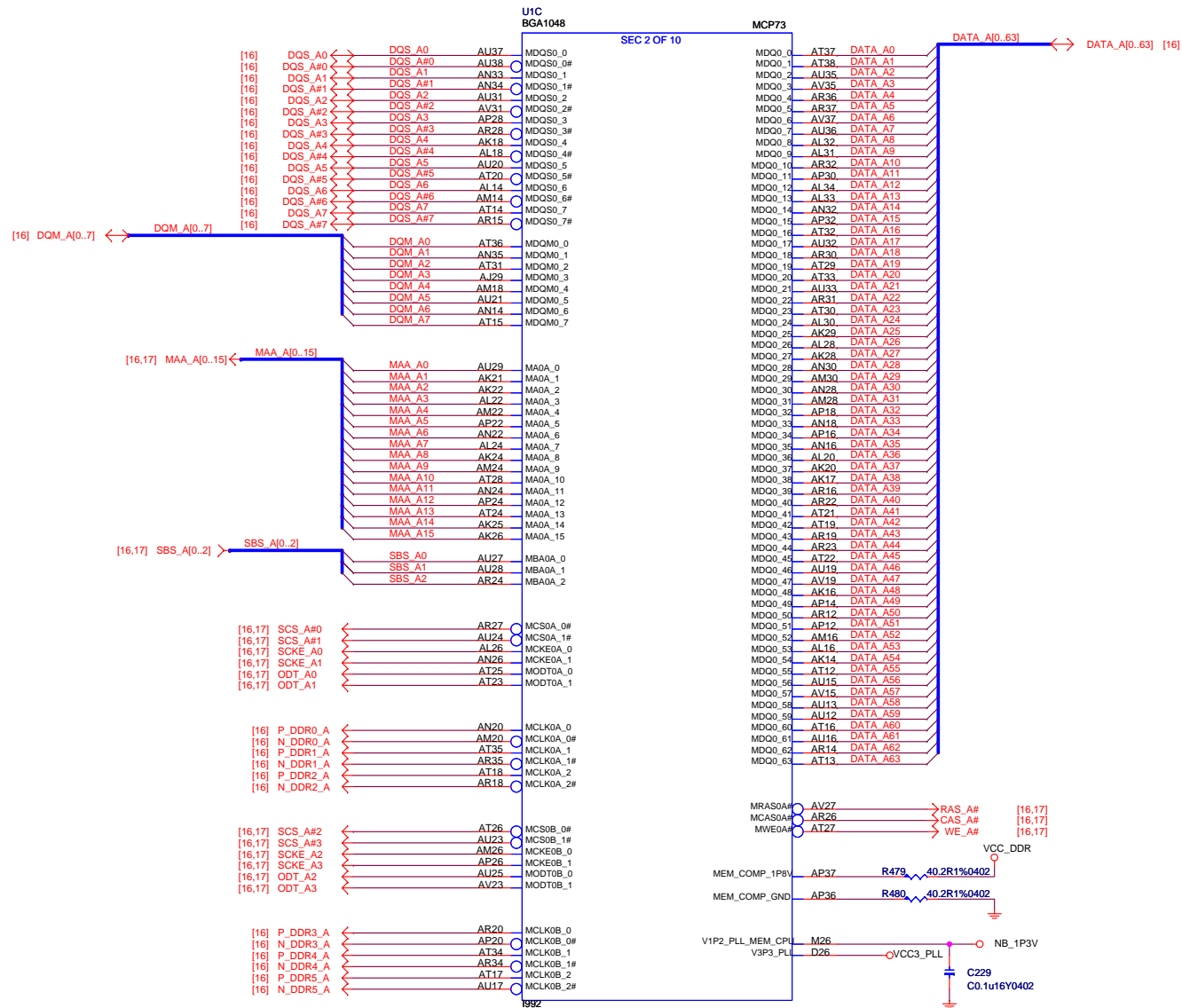
BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	267 MHZ (1067)
0 1 0	200 MHZ (800)
0 0 1	133 MHZ (533)

Prescott / Cedar Mill
 LL_ID[1:0] = 00
 GTLREF_SEL = 0
 VTT_SEL = 1

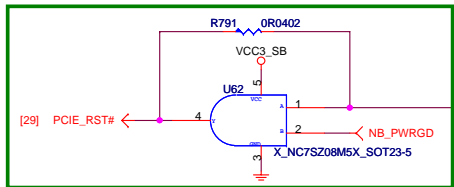
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED



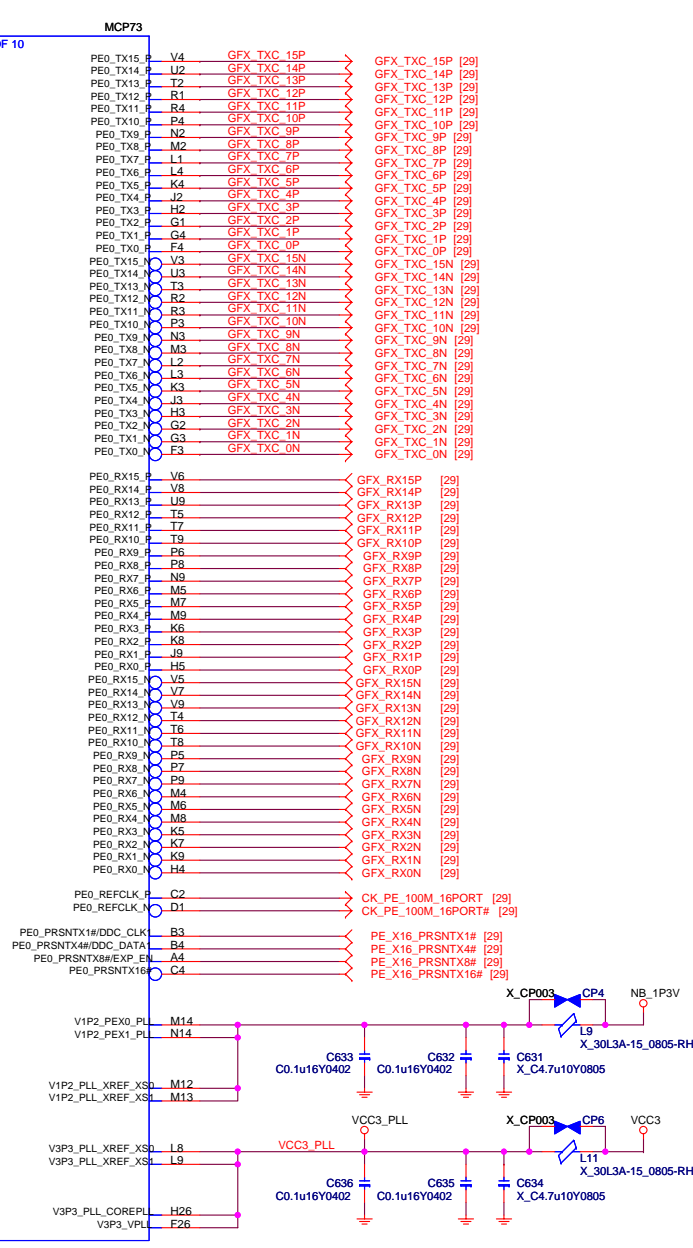
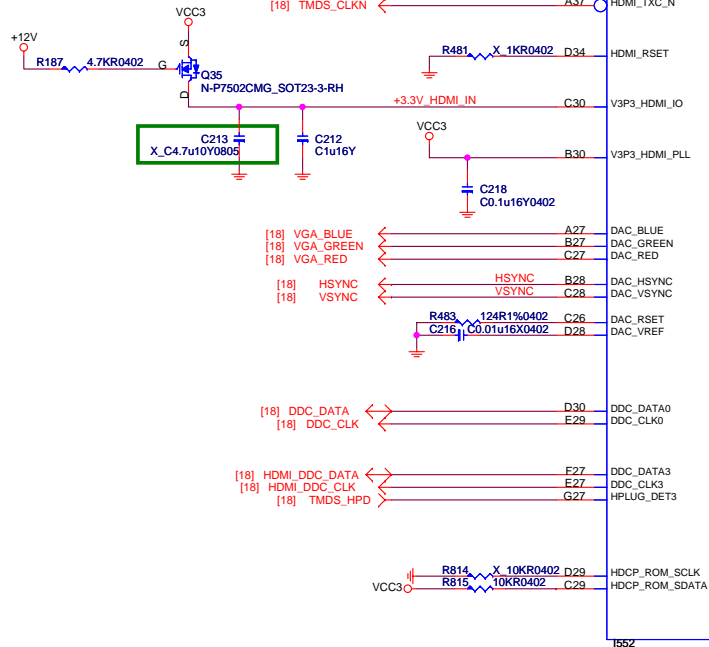


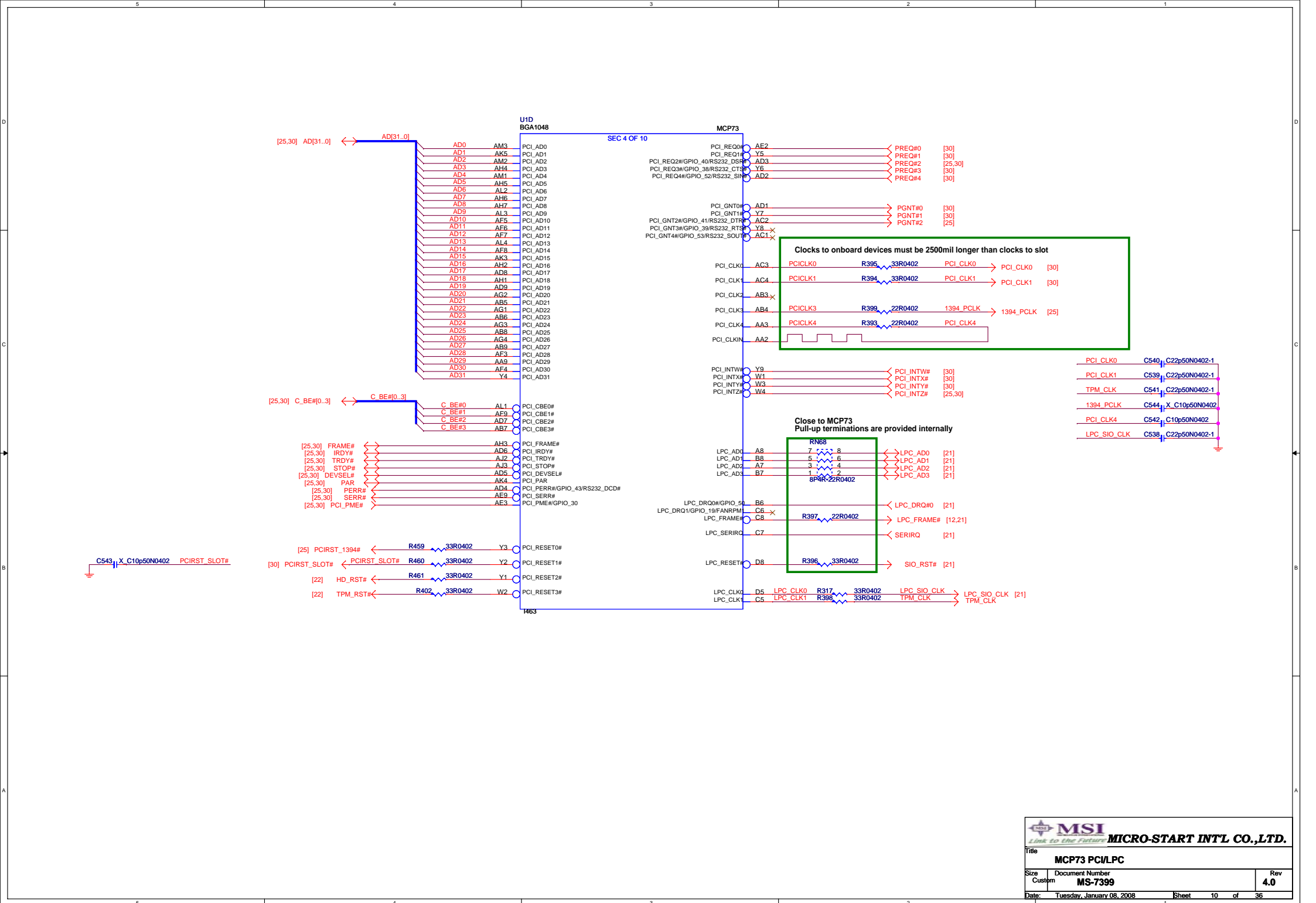


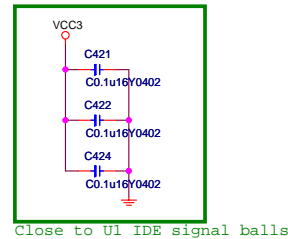
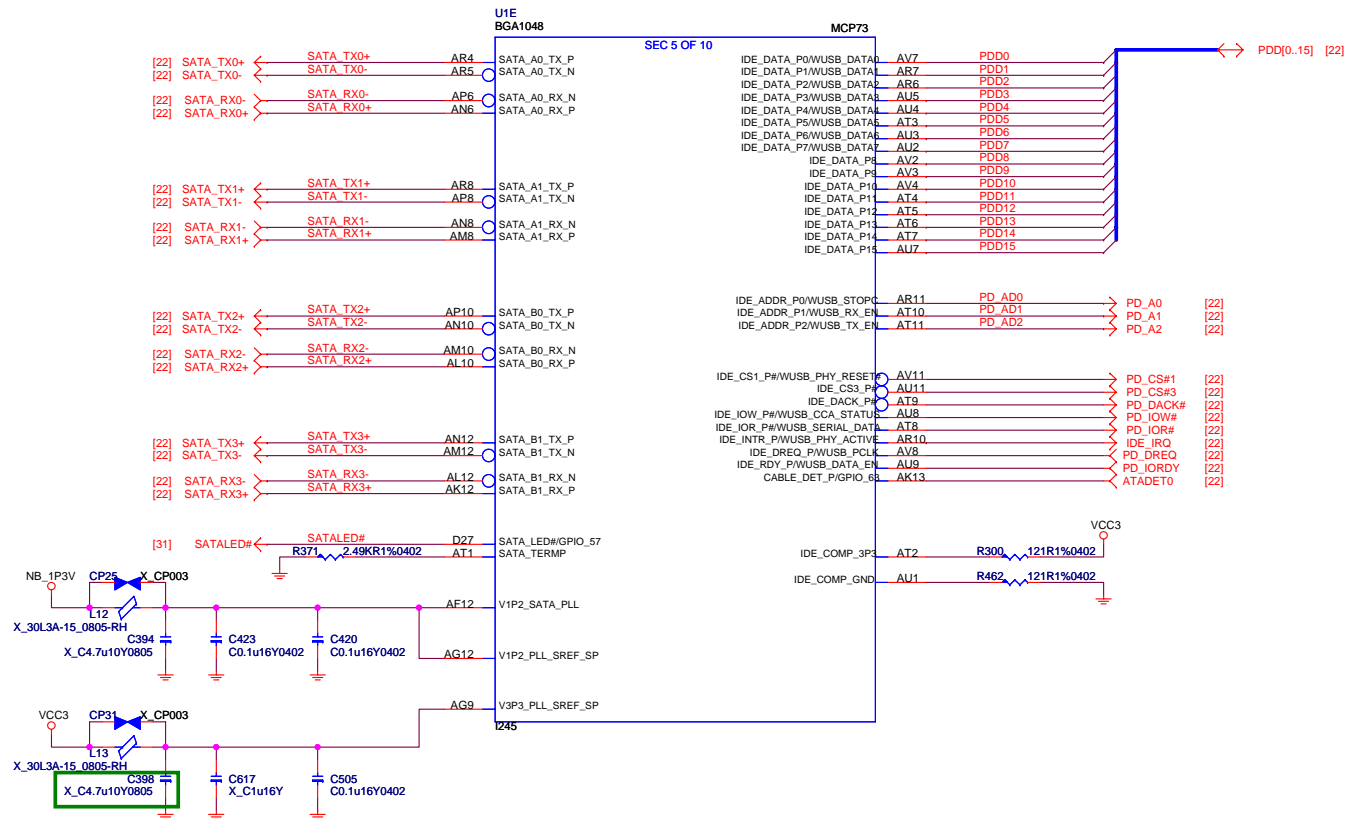
TMDS_00N	R796	158R1%0402	TMDS_00P
TMDS_01N	R797	158R1%0402	TMDS_01P
TMDS_02N	R798	158R1%0402	TMDS_02P
TMDS_CLKN	R799	158R1%0402	TMDS_CLKP



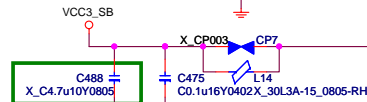
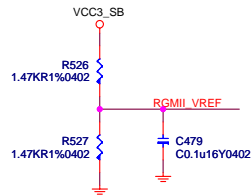
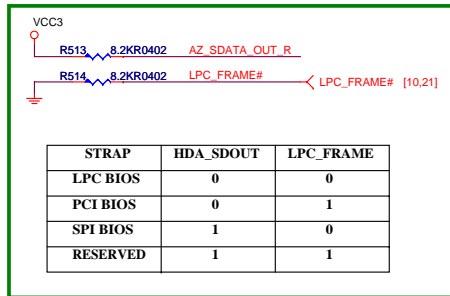
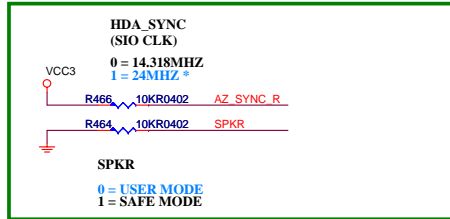
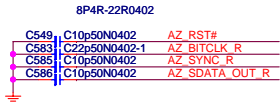
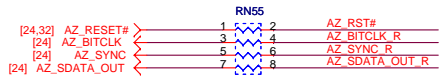
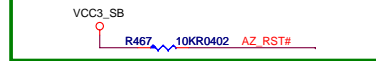
to prevent glitches during power-up



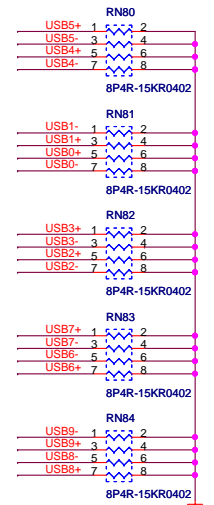
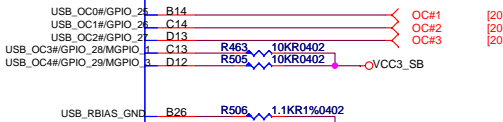
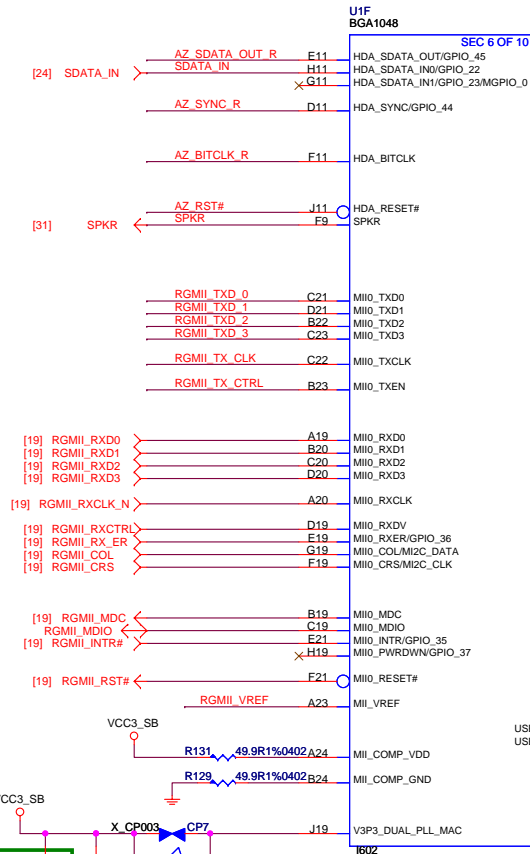
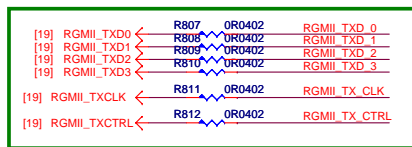


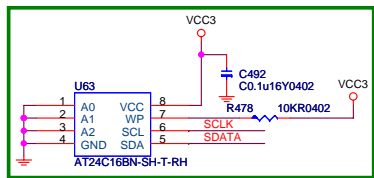


Strapping 10K ohm to VCC3_SB: RGMII

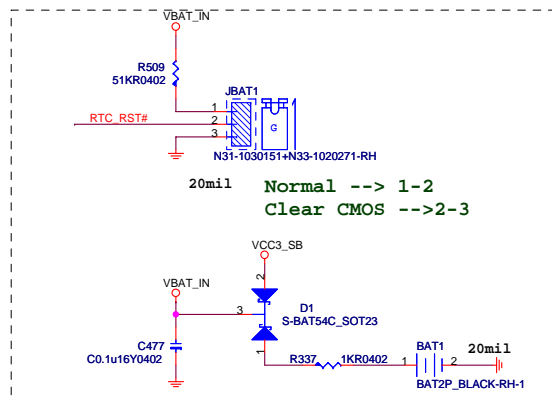
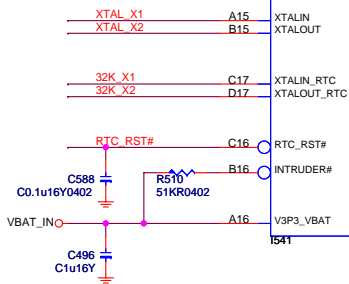
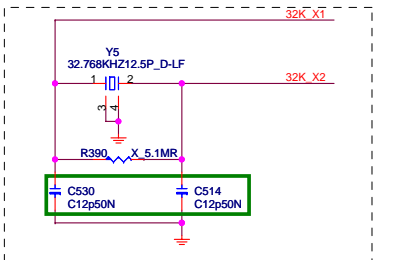
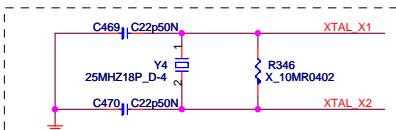
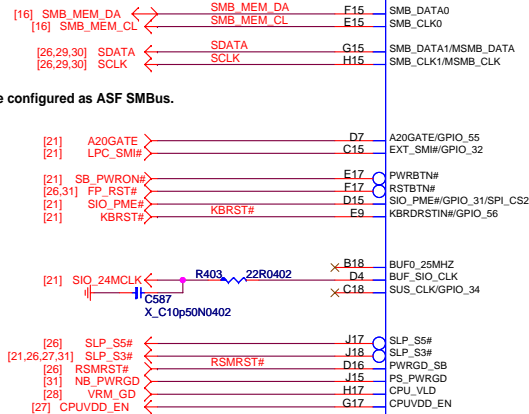
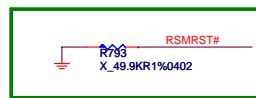
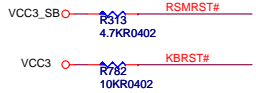


Close to U1

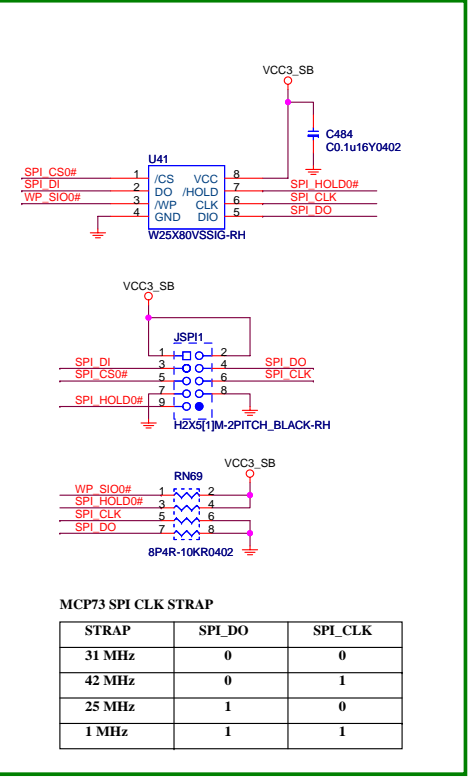
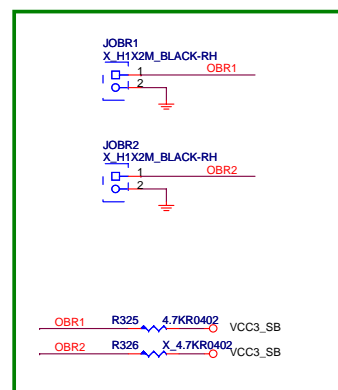
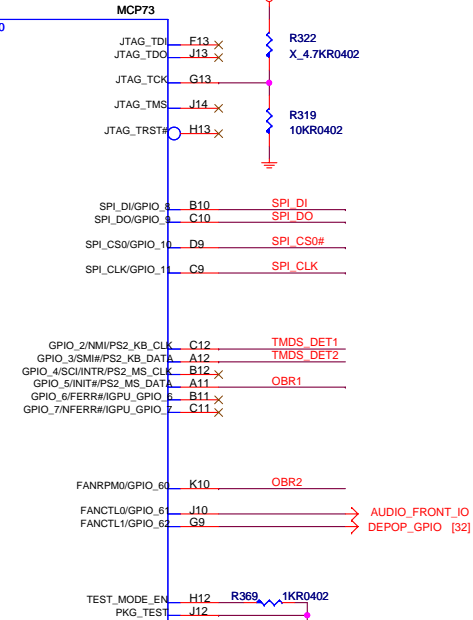




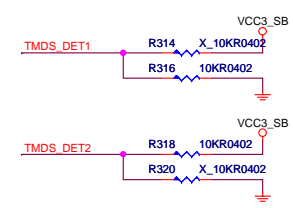
When SDATA/SCLK are not used, it can be configured as ASF SMBus.



20mil Normal --> 1-2
Clear CMOS --> 2-3

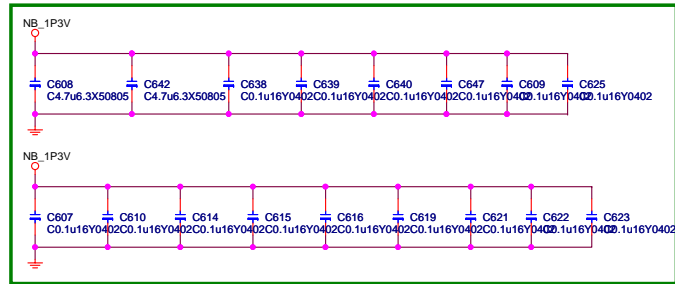


STRAP	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1



HDMI/DVI Detect	TMDs_DET1	TMDs_DET2
DVI	1	0
HDMI	0	1
N/A	0	0

Bottom side



U11	BGA1048
AA12	VIP2_VDD_CORE
AA13	VIP2_VDD_CORE
AA19	VIP2_VDD_CORE
AA21	VIP2_VDD_CORE
AA22	VIP2_VDD_CORE
AA23	VIP2_VDD_CORE
AA24	VIP2_VDD_CORE
AA26	VIP2_VDD_CORE
AB12	VIP2_VDD_CORE
AB13	VIP2_VDD_CORE
AB15	VIP2_VDD_CORE
AB16	VIP2_VDD_CORE
AB17	VIP2_VDD_CORE
AB19	VIP2_VDD_CORE
AB21	VIP2_VDD_CORE
AB26	VIP2_VDD_CORE
AC12	VIP2_VDD_CORE
AC13	VIP2_VDD_CORE
AC17	VIP2_VDD_CORE
AC19	VIP2_VDD_CORE
AC21	VIP2_VDD_CORE
AC23	VIP2_VDD_CORE
AC24	VIP2_VDD_CORE
AC26	VIP2_VDD_CORE
AD12	VIP2_VDD_CORE
AD13	VIP2_VDD_CORE
AD17	VIP2_VDD_CORE
AD19	VIP2_VDD_CORE
AD21	VIP2_VDD_CORE
AD23	VIP2_VDD_CORE
AD26	VIP2_VDD_CORE
AE12	VIP2_VDD_CORE
AE26	VIP2_VDD_CORE
AH8	VIP2_VDD_CORE
AH9	VIP2_VDD_CORE
AJ10	VIP2_VDD_CORE
AJ6	VIP2_VDD_CORE
AJ8	VIP2_VDD_CORE
AJ9	VIP2_VDD_CORE
AK10	VIP2_VDD_CORE
AK6	VIP2_VDD_CORE
AK7	VIP2_VDD_CORE
AK8	VIP2_VDD_CORE
AK9	VIP2_VDD_CORE
AL6	VIP2_VDD_CORE
AL8	VIP2_VDD_CORE
AM4	VIP2_VDD_CORE
AM5	VIP2_VDD_CORE
AM6	VIP2_VDD_CORE
AN2	VIP2_VDD_CORE
AN3	VIP2_VDD_CORE
AN4	VIP2_VDD_CORE
AP3	VIP2_VDD_CORE
AP4	VIP2_VDD_CORE
AR1	VIP2_VDD_CORE
AR2	VIP2_VDD_CORE
AR3	VIP2_VDD_CORE
M23	VIP2_VDD_CORE
M24	VIP2_VDD_CORE
M25	VIP2_VDD_CORE
N23	VIP2_VDD_CORE
N24	VIP2_VDD_CORE
N25	VIP2_VDD_CORE
N26	VIP2_VDD_CORE
P26	VIP2_VDD_CORE
R18	VIP2_VDD_CORE
R20	VIP2_VDD_CORE
R22	VIP2_VDD_CORE
R24	VIP2_VDD_CORE
R26	VIP2_VDD_CORE
T18	VIP2_VDD_CORE
T20	VIP2_VDD_CORE
T22	VIP2_VDD_CORE
T26	VIP2_VDD_CORE
U18	VIP2_VDD_CORE
U20	VIP2_VDD_CORE
U22	VIP2_VDD_CORE
U23	VIP2_VDD_CORE
U24	VIP2_VDD_CORE
U26	VIP2_VDD_CORE
V15	VIP2_VDD_CORE
V16	VIP2_VDD_CORE
V17	VIP2_VDD_CORE
V18	VIP2_VDD_CORE
V20	VIP2_VDD_CORE
V26	VIP2_VDD_CORE
W20	VIP2_VDD_CORE
W21	VIP2_VDD_CORE
W22	VIP2_VDD_CORE
W23	VIP2_VDD_CORE
W24	VIP2_VDD_CORE
W26	VIP2_VDD_CORE
Y12	VIP2_VDD_CORE
Y13	VIP2_VDD_CORE
Y15	VIP2_VDD_CORE
Y16	VIP2_VDD_CORE
Y17	VIP2_VDD_CORE
Y18	VIP2_VDD_CORE
Y19	VIP2_VDD_CORE
Y26	VIP2_VDD_CORE

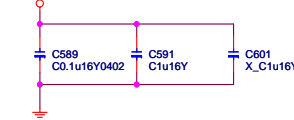
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SEC 8 OF 10

MCP73	V_FSB_VTT
VIP2_CPU_VTT	A31
VIP2_CPU_VTT	A32
VIP2_CPU_VTT	B27
VIP2_CPU_VTT	AD27
VIP2_CPU_VTT	B31
VIP2_CPU_VTT	B32
VIP2_CPU_VTT	C31
VIP2_CPU_VTT	C32
VIP2_CPU_VTT	C33
VIP2_CPU_VTT	D31
VIP2_CPU_VTT	D32
VIP2_CPU_VTT	D33
VIP2_CPU_VTT	E31
VIP2_CPU_VTT	F29
VIP2_CPU_VTT	F30
VIP2_CPU_VTT	F31
VIP2_CPU_VTT	G29
VIP2_CPU_VTT	H27
VIP2_CPU_VTT	H28
VIP2_CPU_VTT	H29
VIP2_CPU_VTT	J27
VIP2_CPU_VTT	J28
VIP2_CPU_VTT	J29
VIP2_CPU_VTT	K29
VIP2_CPU_VTT	M27
VIP2_CPU_VTT	N27
VIP2_CPU_VTT	P27
VIP2_CPU_VTT	T27
VIP2_CPU_VTT	V27
VIP2_CPU_VTT	Y27

V_FSB_VTT

V_FSB_VTT



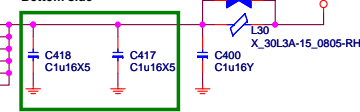
	NB_1P3V
V1P2_PEX_DVDD	N13
V1P2_PEX_DVDD	R15
V1P2_PEX_DVDD	R16
V1P2_PEX_DVDD	T15
V1P2_PEX_DVDD	T16

VIP2_PEX_AVDD	N12
VIP2_PEX_AVDD	P12
VIP2_PEX_AVDD	P13
VIP2_PEX_AVDD	T12
VIP2_PEX_AVDD	T13
VIP2_PEX_AVDD	U12
VIP2_PEX_AVDD	U13
VIP2_PEX_AVDD	W12
VIP2_PEX_AVDD	W13

			NB_1P3V	
V1P2_SATA_DVDD	AD15			C200
V1P2_SATA_DVDD	AF15			
V1P2_SATA_DVDD	AF16			
V1P2_SATA_DVDD	AG16			

Bottom side

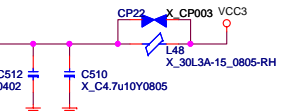
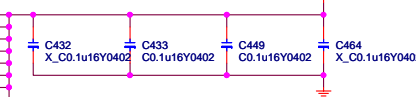
V1P2_SATA_AVDD0	AE13
V1P2_SATA_AVDD0	AE13
V1P2_SATA_AVDD0	AE14
V1P2_SATA_AVDD0	AG13
V1P2_SATA_AVDD0	AG14
V1P2_SATA_AVDD0	AG15



V3P3	AC6
V3P3	AC8
V3P3	AC9
V3P3	AG6
V3P3	AG8
V3P3	W6
V3P3	W8
V3P3	W9

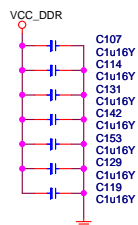
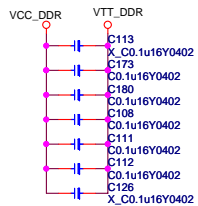
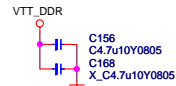
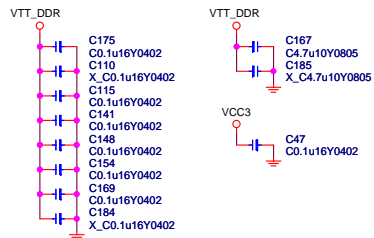
V3P3_DAC F28

C512
C0.1uF

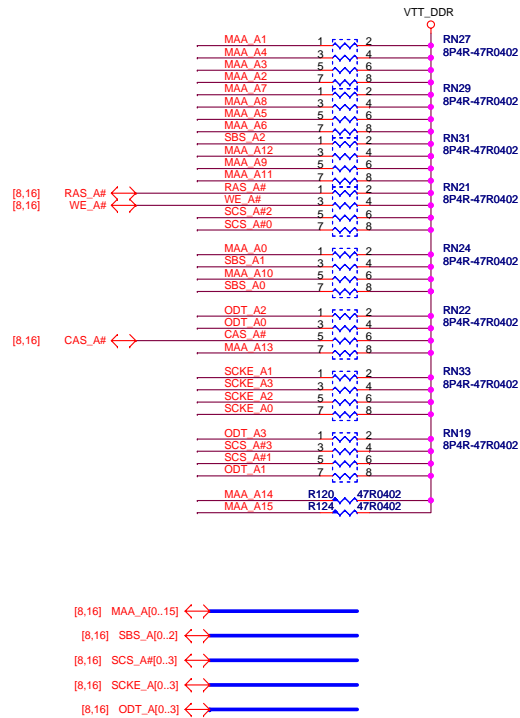


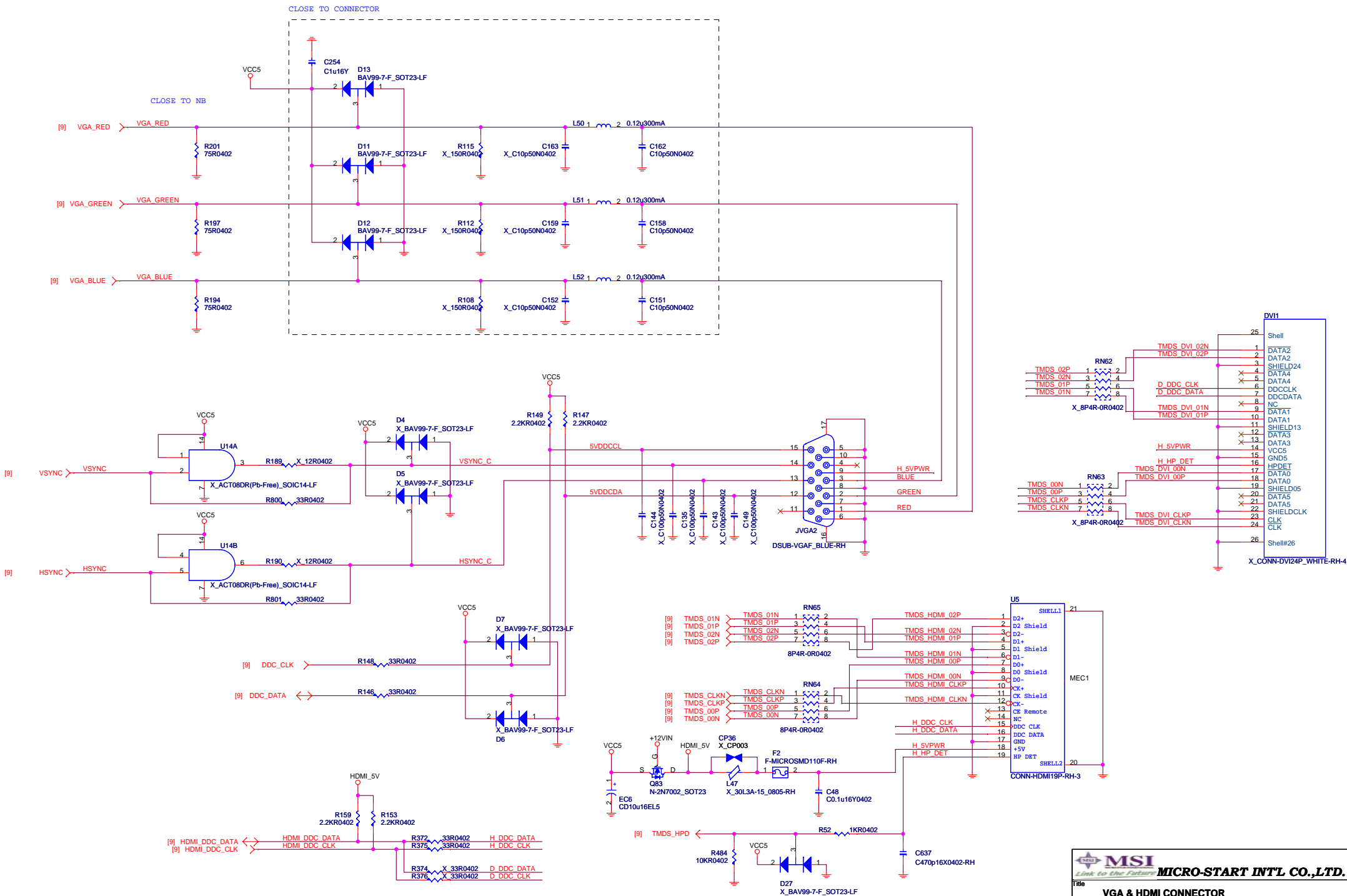
MICRO-START INT'L CO.,LTD.			
Title			
MCP73 CORE/VTT POWER			
Size	Document Number	Rev	
Custom	MS-7399	4.0	
Date:	Tuesday, January 08, 2008	Sheet	14 of 36

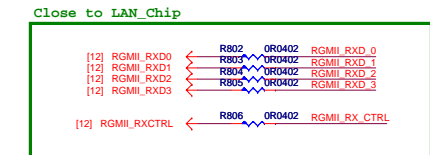
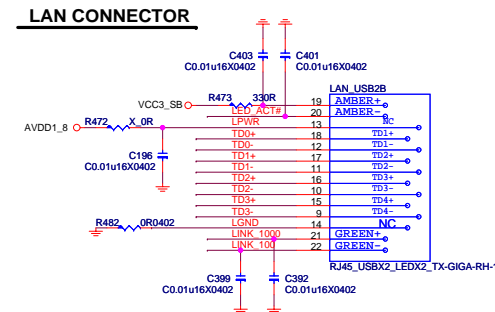
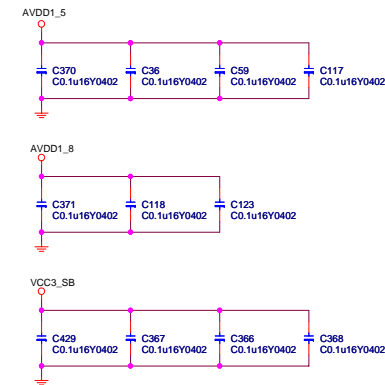
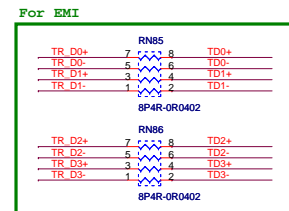
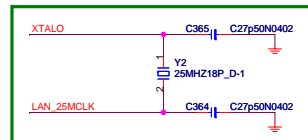
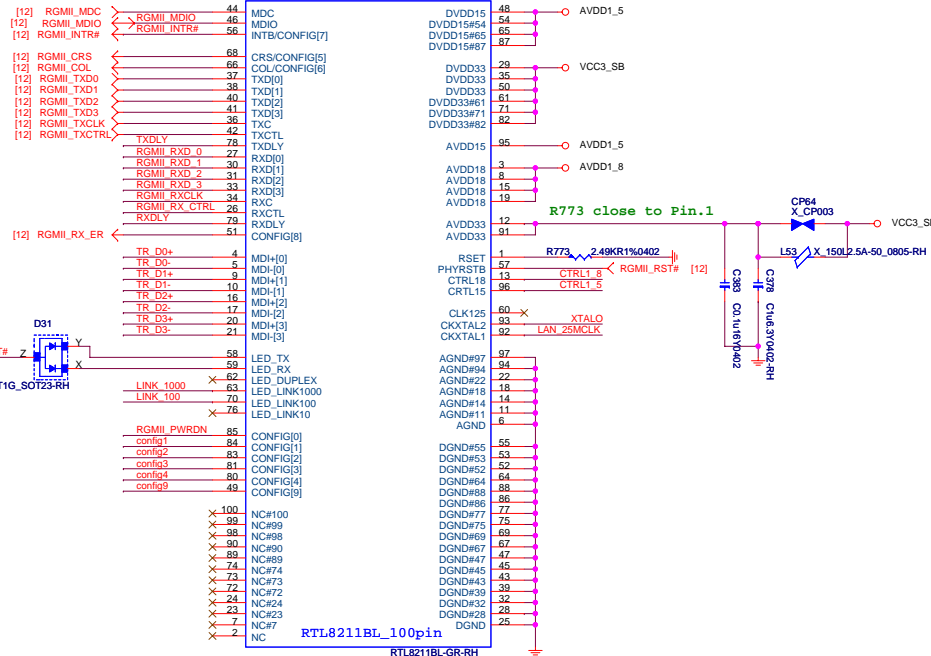
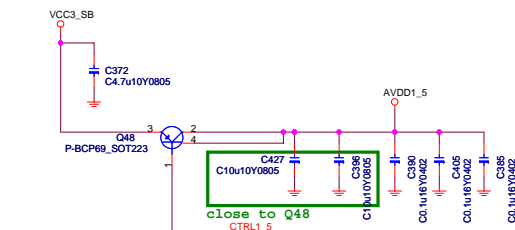
CHANNEL A VTT_DDR
DECOUPLING CAPS



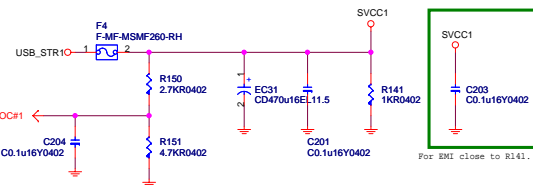
DDR II TERMINATION



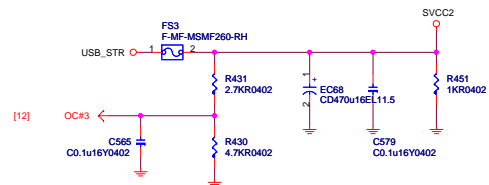




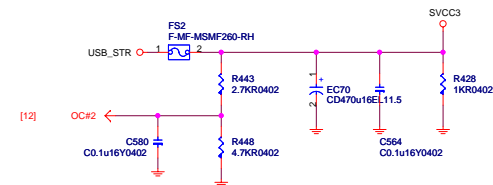
POWER CIRCUIT FOR USB PORT 0,1,2,3



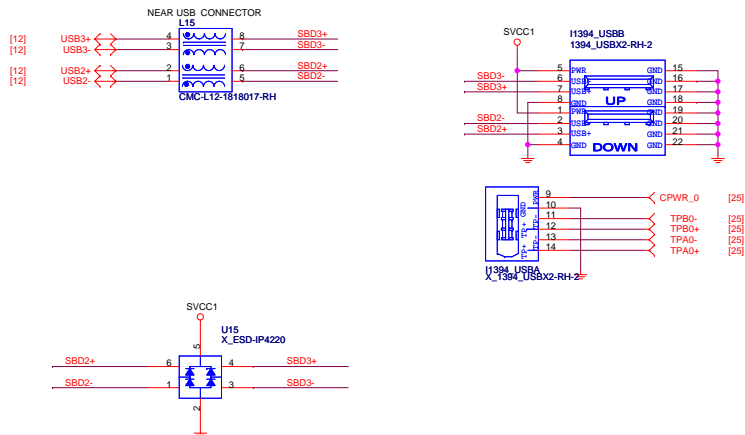
POWER CIRCUIT FOR USB PORT 4,5,6,7



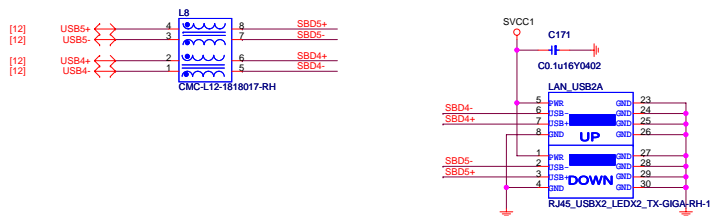
POWER CIRCUIT FOR USB PORT 8,9



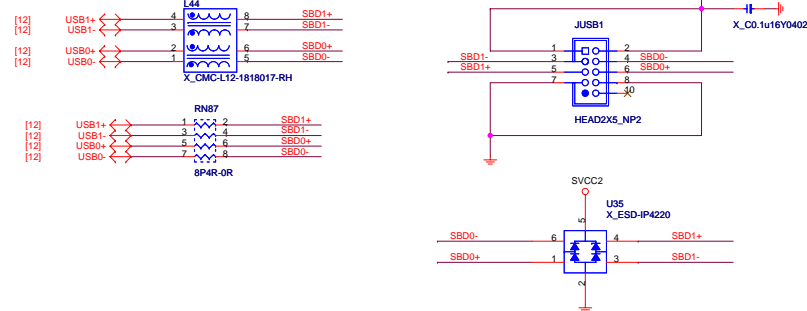
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



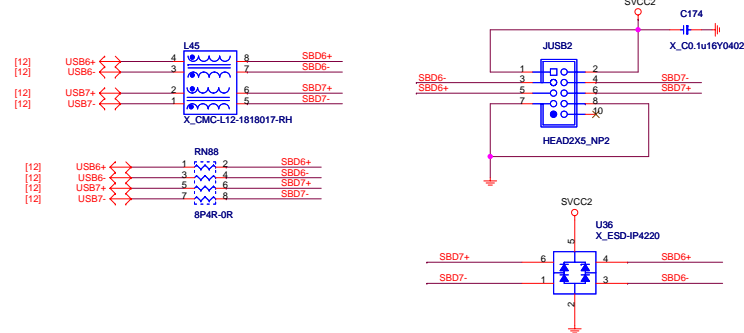
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



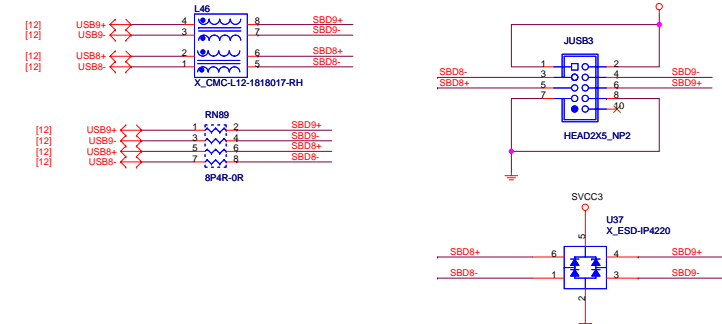
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



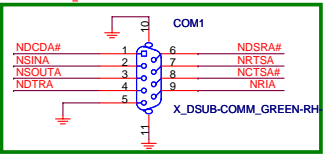
USB CARD READER + IR MODULE FOR USB PORT 8,9



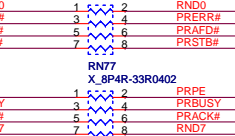
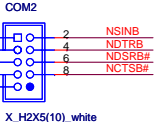
[11] PDD[0..15] \longleftrightarrow



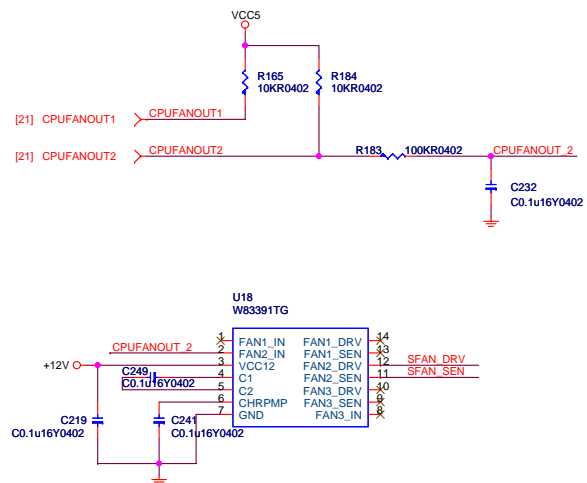
SATA1



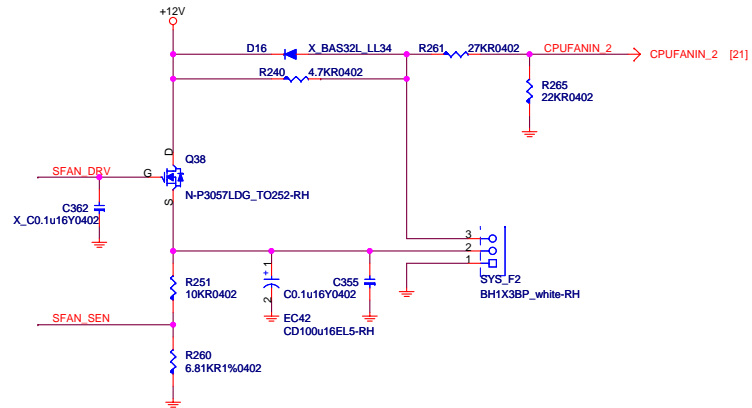
C361..X C01u16Y0402



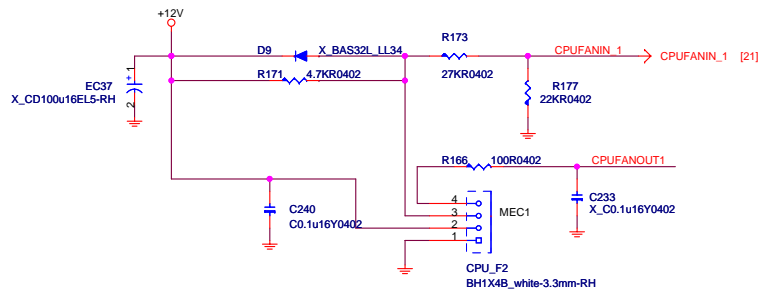
PWM FAN CONTROL



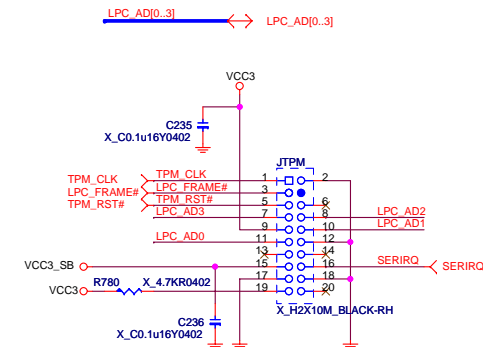
SYS FAN



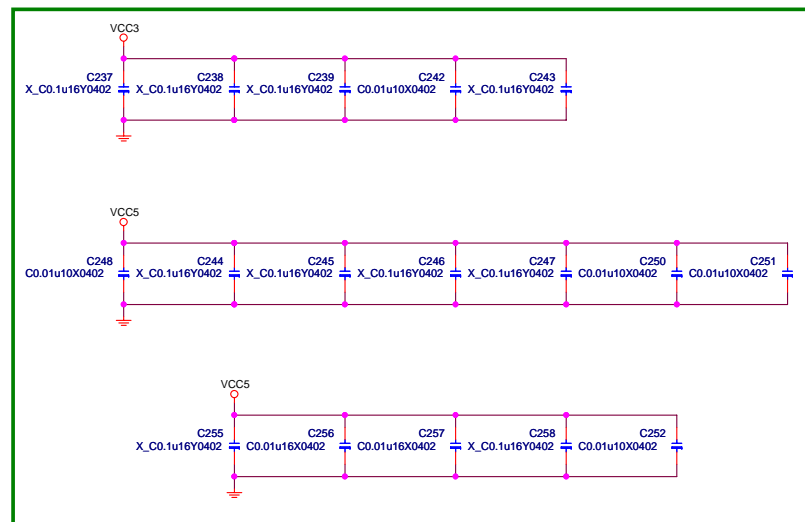
CPU FAN

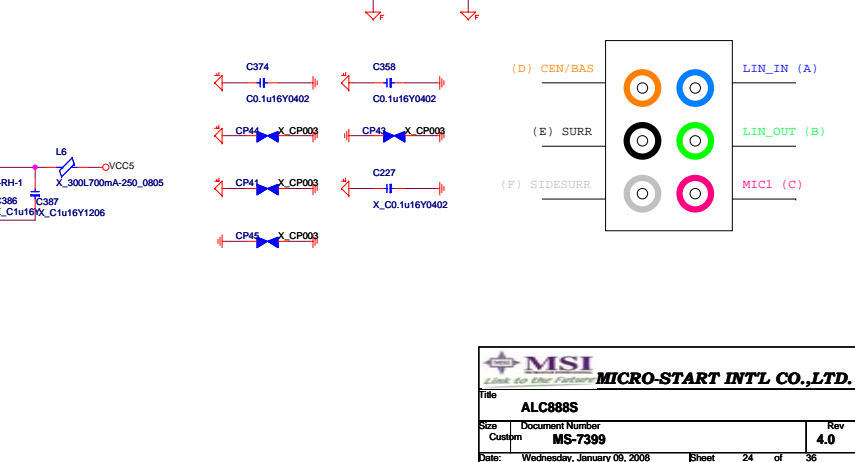
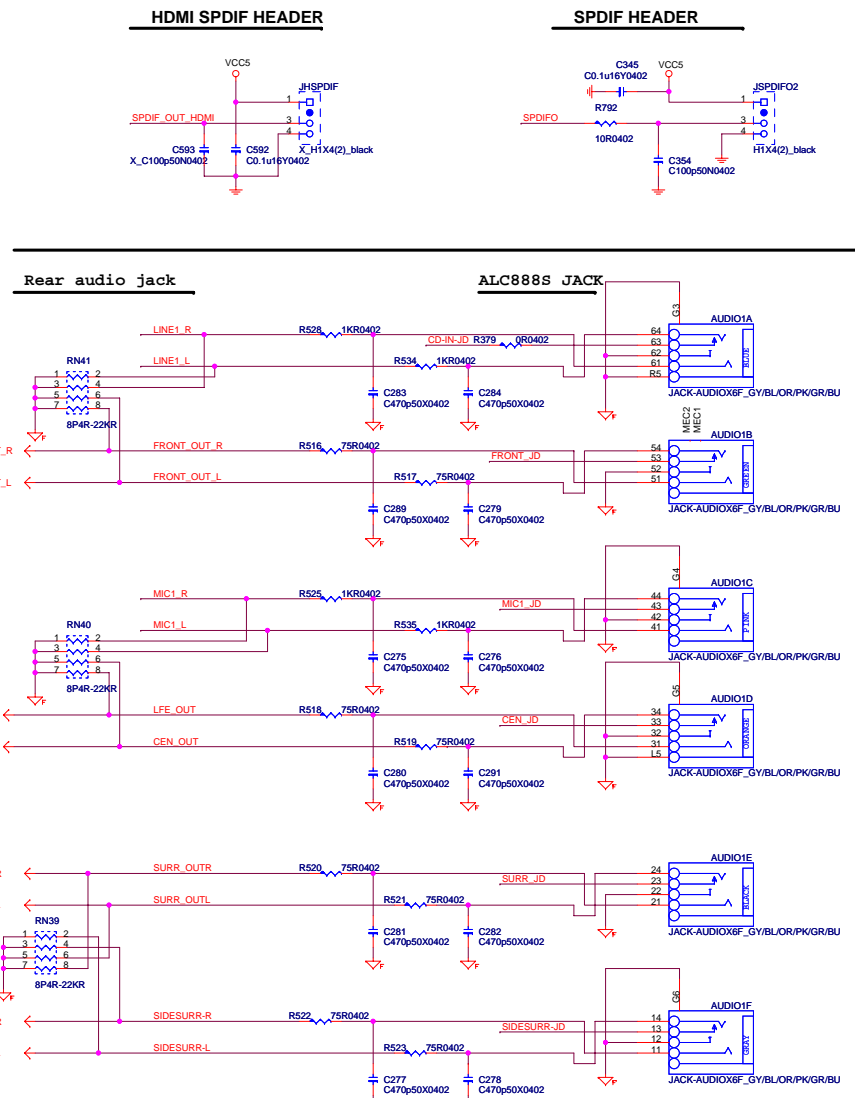
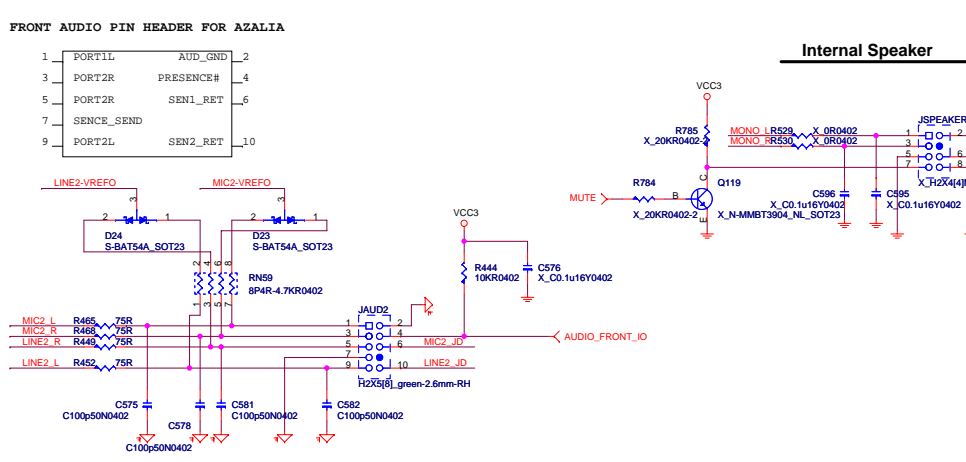
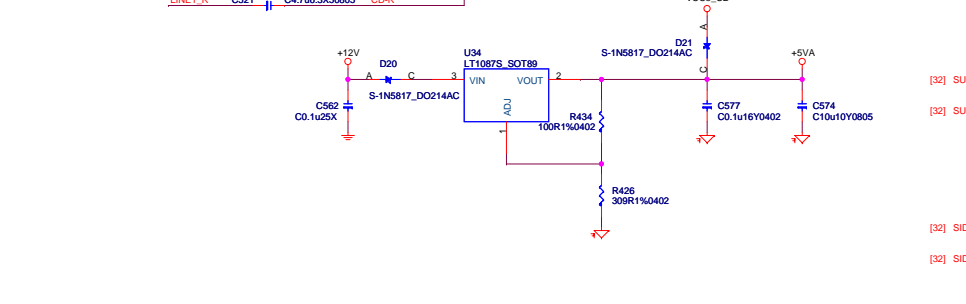
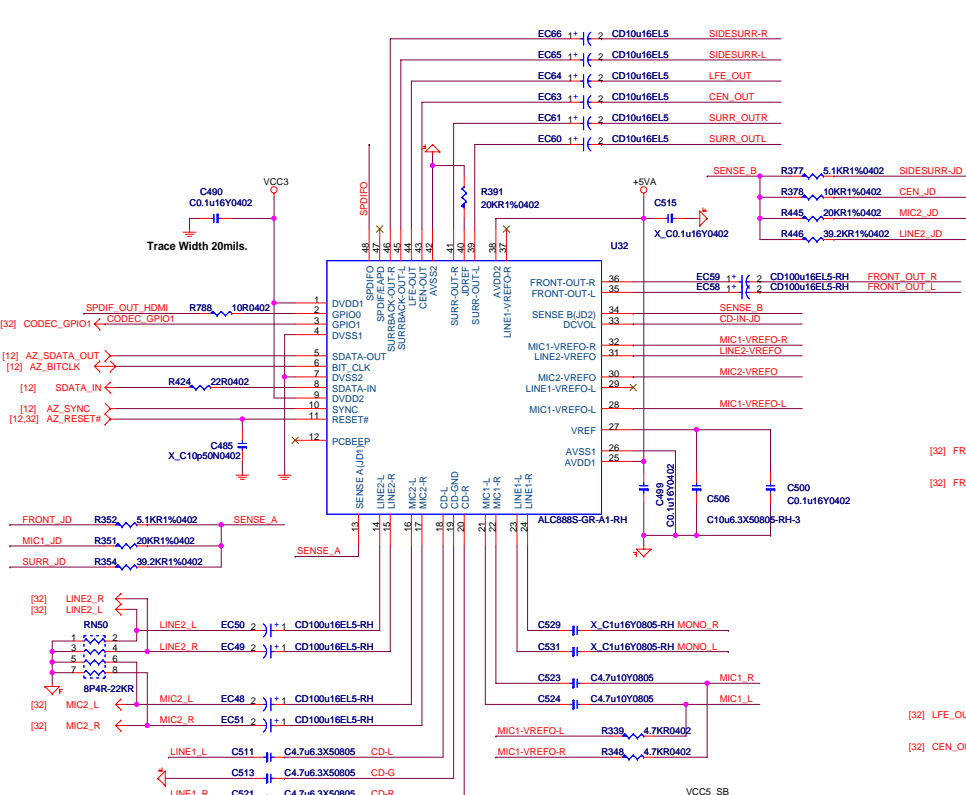


TPM Header



For EMI





3VSB MODE SELECT	
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

[illegible]

The schematic diagram shows the W83310DG SOP8-RH chip with the following connections:

- Pin 1 (VIN):** Connected to VCC_DDR through capacitor EC34 (X_CD1000u63EL15-RH).
- Pin 2 (GND2):** Connected to ground through capacitor C226 (X_C0.1u16Y0402).
- Pin 3 (VREF1):** Connected to ground through capacitor EC30 (X_CD1000u63EL15-RH).
- Pin 4 (VOUT):** Connected to ground through capacitor EC32 (X_CD1000u63EL15-RH).
- Pin 5 (BOOT_SEL):** Connected to ground through capacitor C245 (X_C0.1u16Y0402).
- Pin 6 (VCTRL):** Connected to ground through capacitor C214 (X_C0.1u16Y0402).
- Pin 7 (ENABLE):** Connected to VCC3 through capacitor EC45 (X_CD1000u63EL15-RH).
- Pin 8 (VREF2):** Connected to VCC3 through capacitor EC57 (X_CD1000u63EL15-RH).
- Pin 9 (GND9):** Connected to ground through capacitor C225 (X_C0.1u16Y0402).

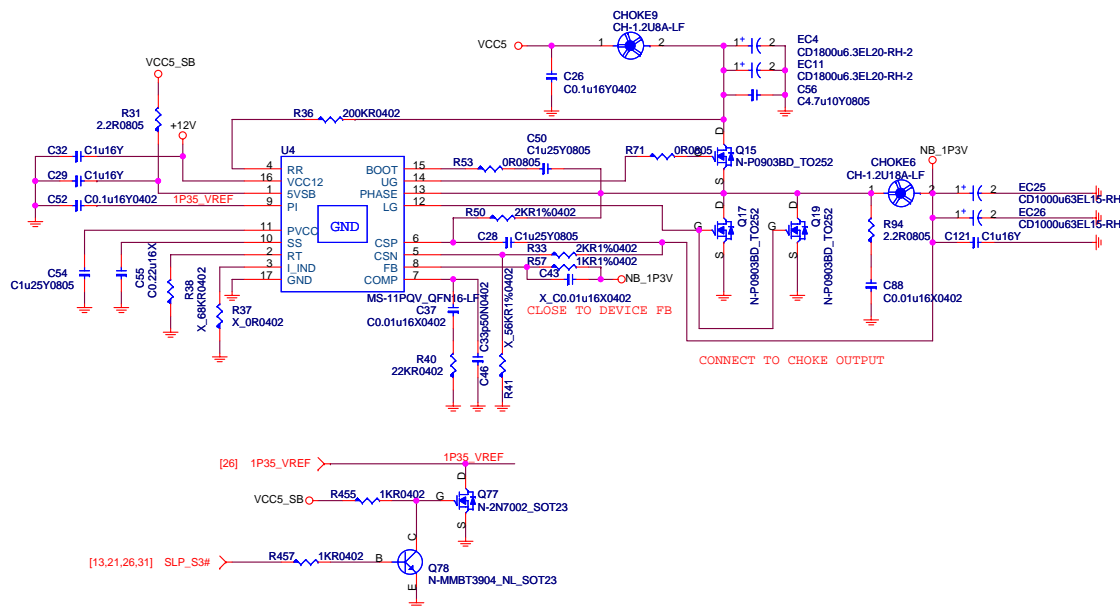
Additional components and connections include:

- VCC3_SB:** Connected to Pin 8 (VREF2) through capacitor C225.
- VCC_DDR:** Connected to Pin 1 (VIN) through capacitor EC34.
- VCC5:** Connected to Pin 7 (ENABLE) through capacitor EC45.
- VCC3:** Connected to Pin 8 (VREF2) through capacitor EC57.
- EC34:** X_CD1000u63EL15-RH
- C226:** X_C0.1u16Y0402
- EC30:** X_CD1000u63EL15-RH
- EC32:** X_CD1000u63EL15-RH
- C245:** X_C0.1u16Y0402
- C214:** X_C0.1u16Y0402
- EC45:** X_CD1000u63EL15-RH
- EC57:** X_CD1000u63EL15-RH
- C225:** X_C0.1u16Y0402
- R163:** 1KR1%0402
- R170:** 1KR1%0402

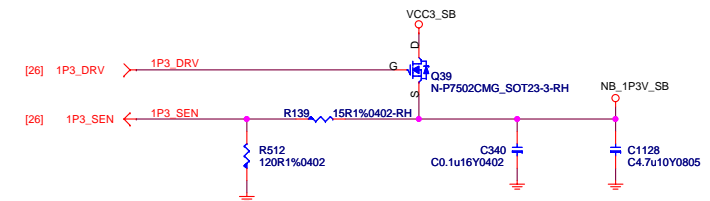
NB 1.3V CORE POWER

(1.3V--8.776A+V_FSB_VTT---5.6A=14.376)

The Ripple Current For V_1P25_CORE:
 $Duty = (1.35V/5V) * (100\%/80\%) = 0.3375$ (Efficiency: 80%)
 $I_{rms} = I_o * \{ [Duty * (1 - Duty)]^{0.5} \}$
 $= 14.4 * \{ [0.27 * 0.73]^{0.5} \} = 6.393$ (A)
 Rated Ripple Current (65 degree): $1800mA * 2.3 * 2 = 8.28A > 6.393A$

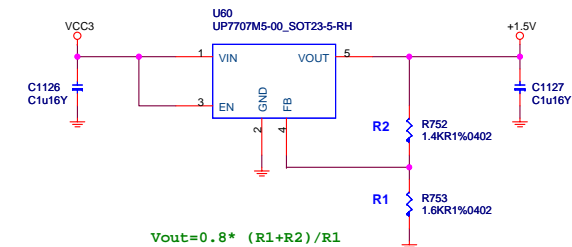


NB 1.3VSB POWER 25mA

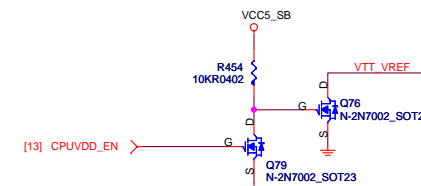
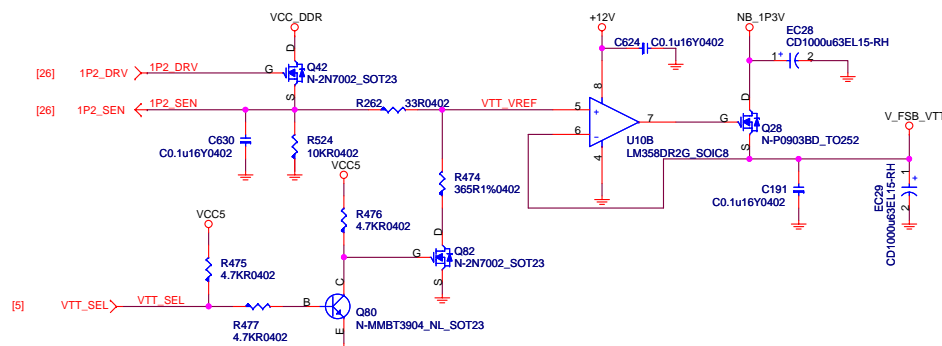


+1.5V POWER

up7707: 600mA Low Dropout Linear Regulator

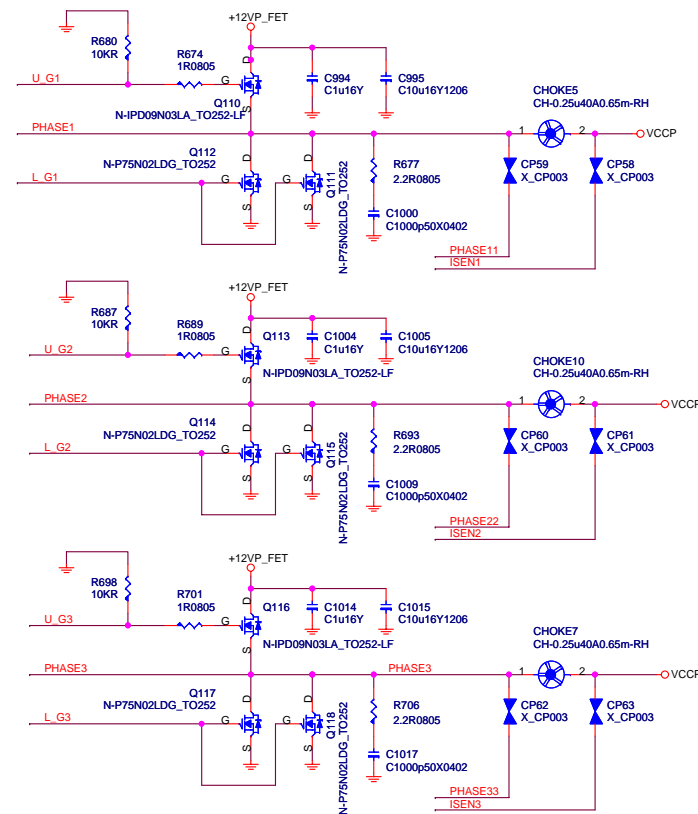
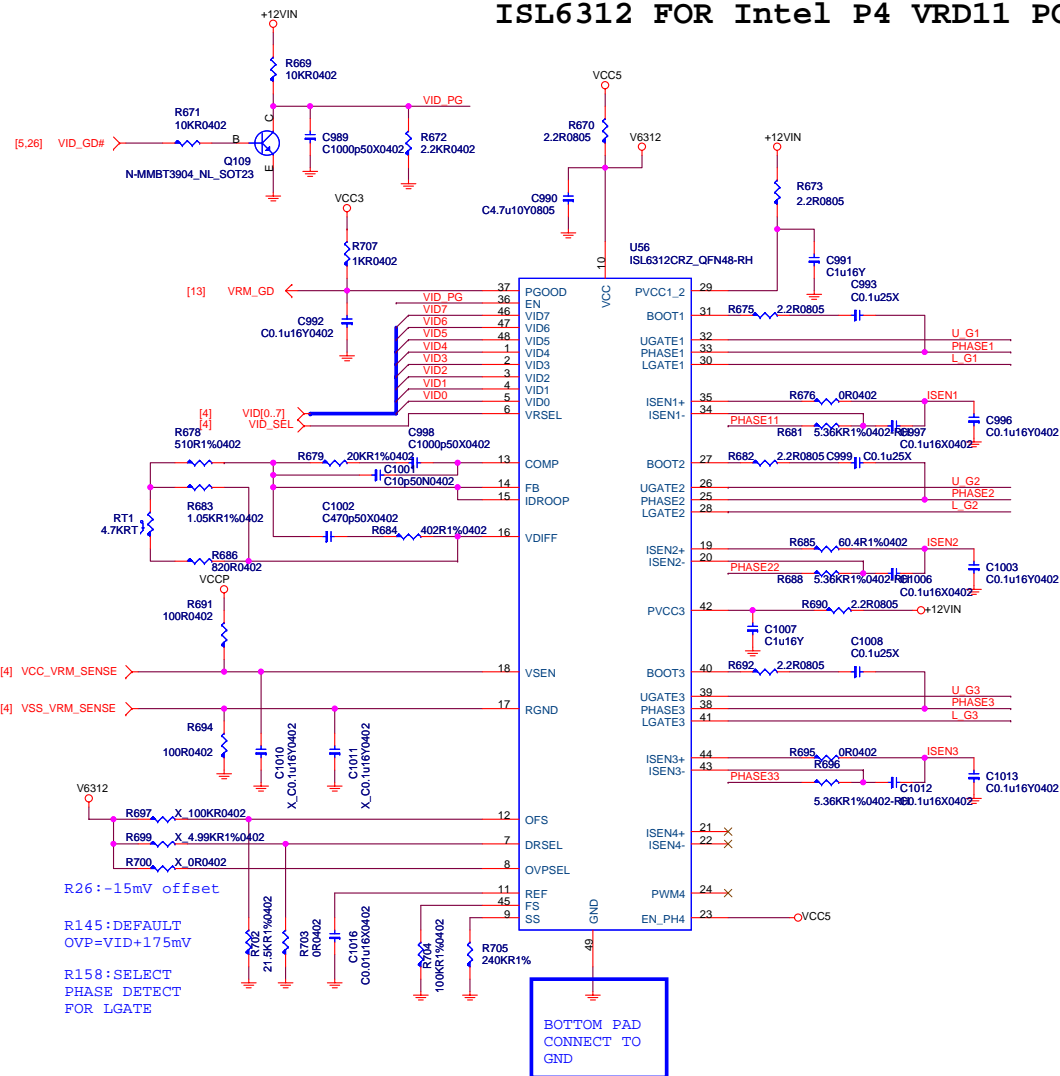


CPU FSB VTT POWER

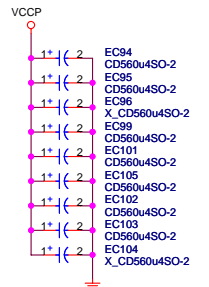


VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

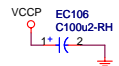
ISL6312 FOR Intel P4 VRD11 POWER CKT



OS-CON Capacitors

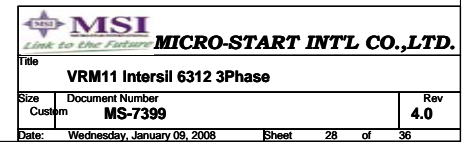
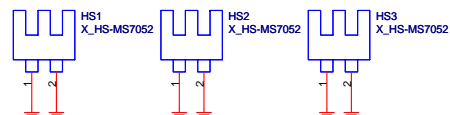
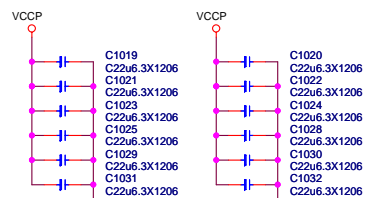


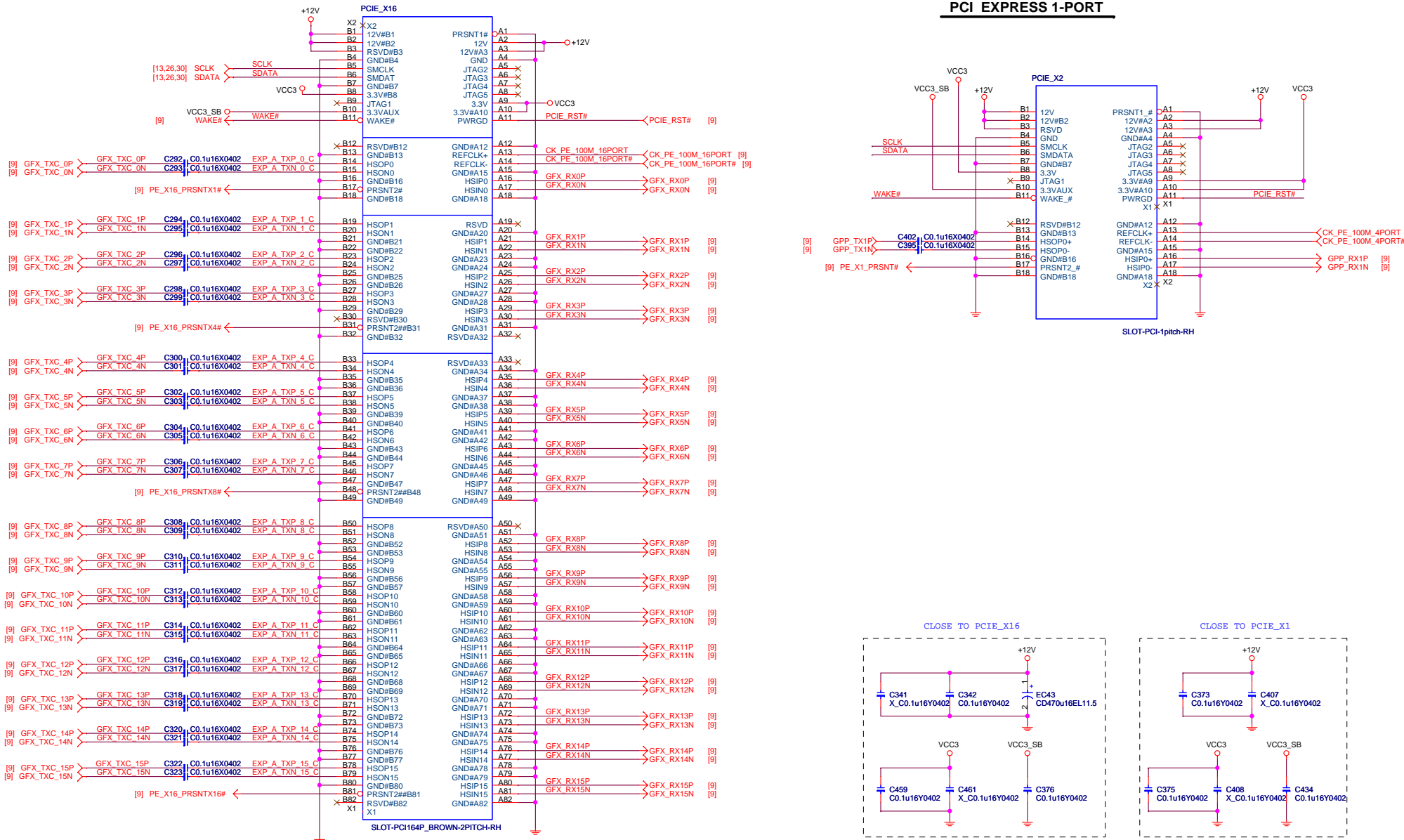
SP Capacitors



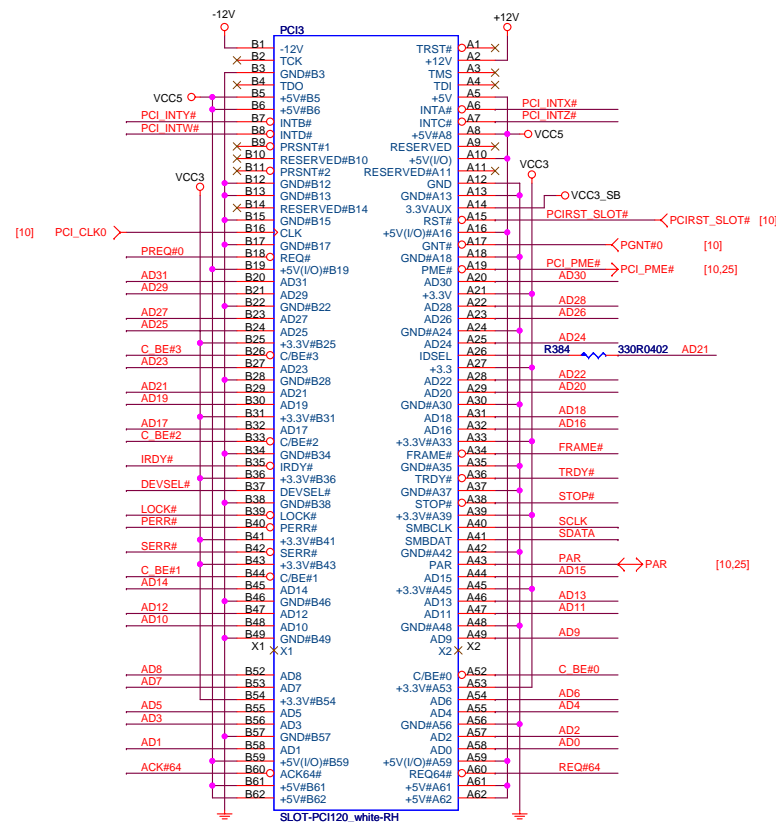
CPU DECOUPLING CAPACITORS

Place these caps within socket cavity



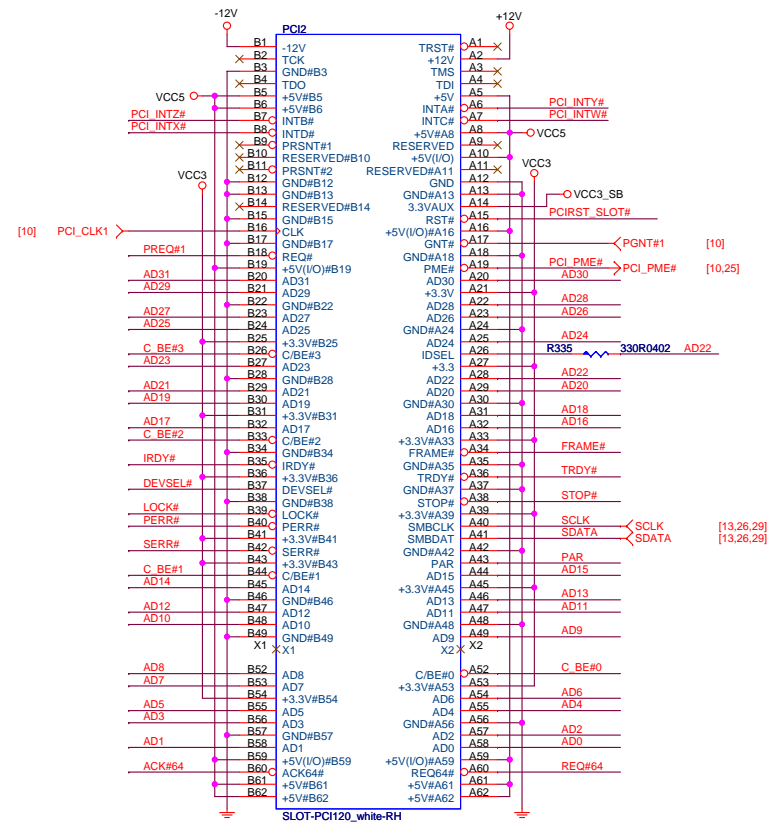


PCI SLOT 1 (PCI VER: 2.3 COMPLY)



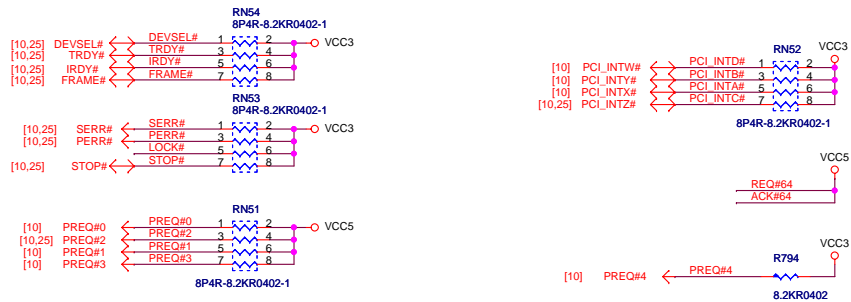
IDSEL = AD21
MASTER = PREQ#0
PCI_INTX#

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

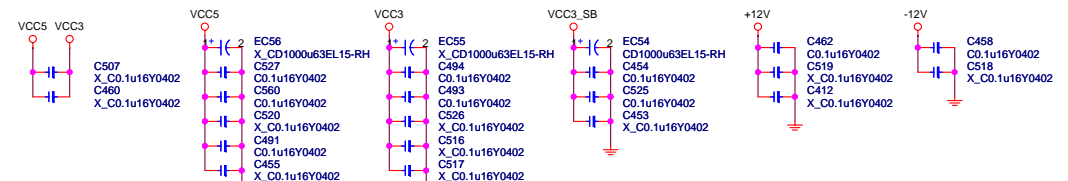


IDSEL = AD22
MASTER = PREQ#1
PCI_INTX#

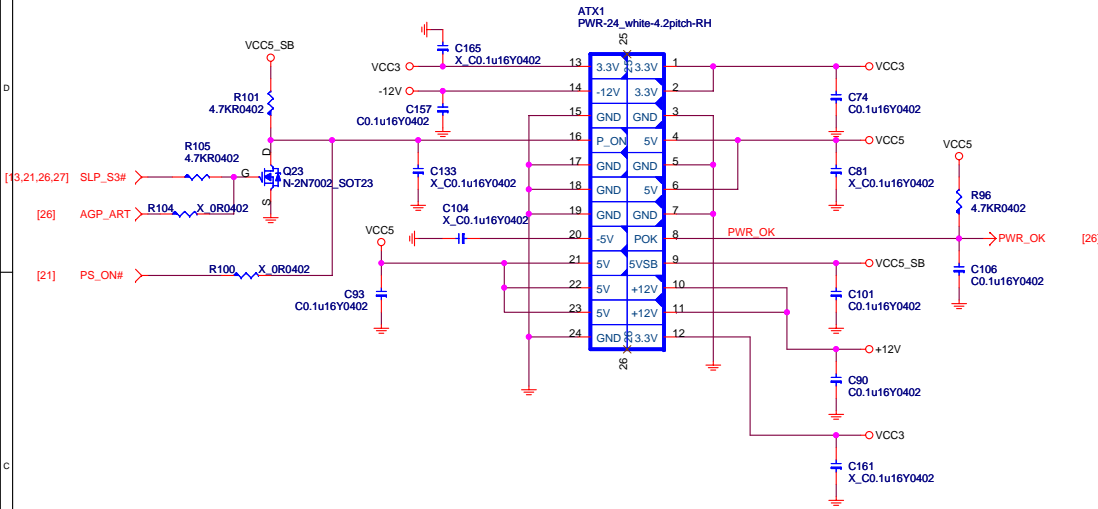
PCI PULL-UP / DOWN RESISTORS



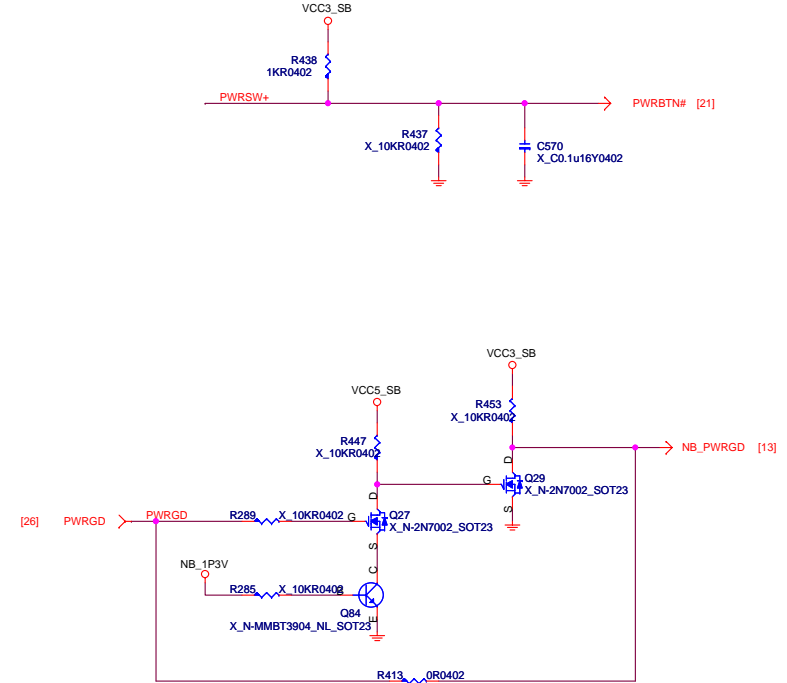
PCI SLOT DECOUPLING CAPACITORS



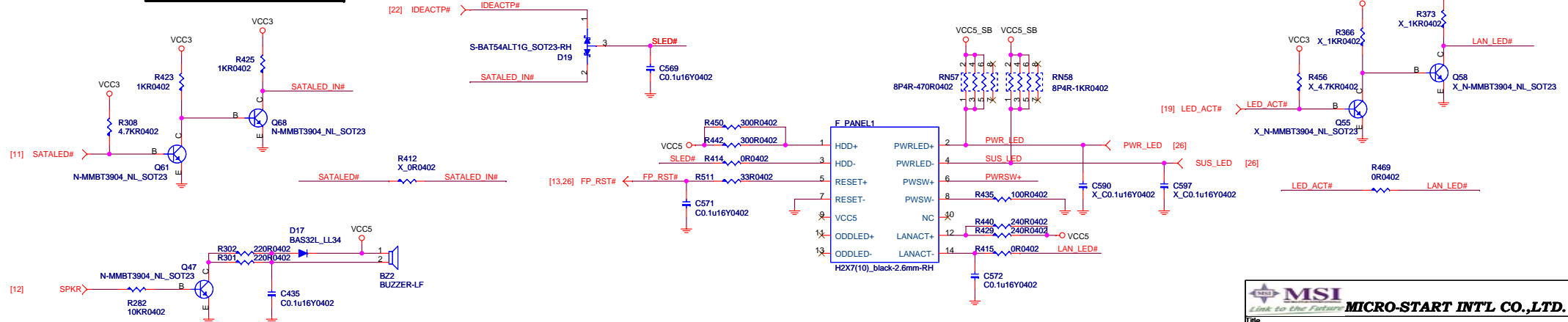
ATX CONNECTOR



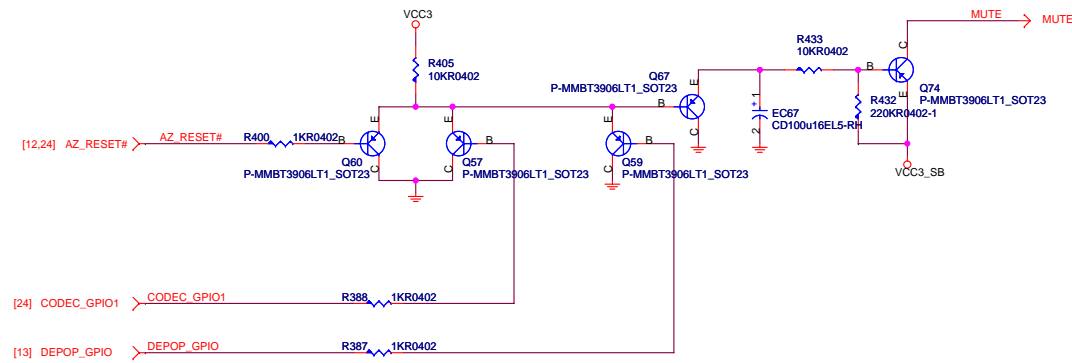
POWER BUTTON



acer Front Panel Connector



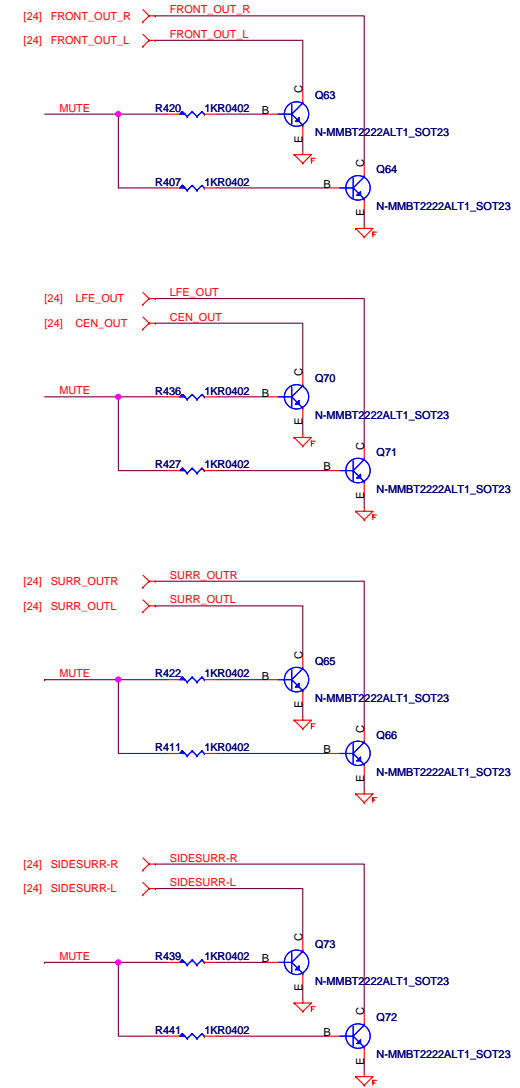
Audio De-Pop Control Circuit



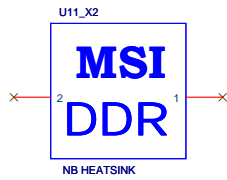
Front Audio Port De-Pop Circuit



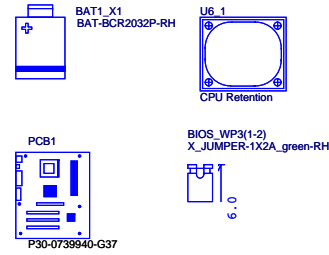
Rear Audio Port De-Pop Circuit



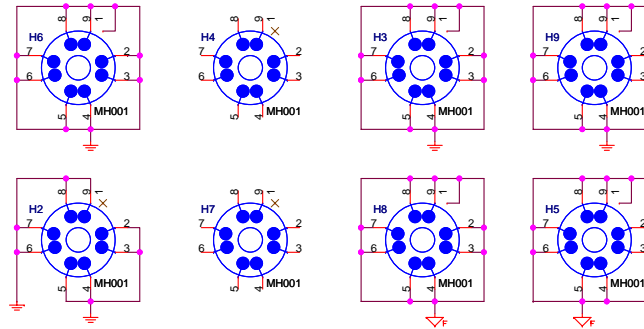
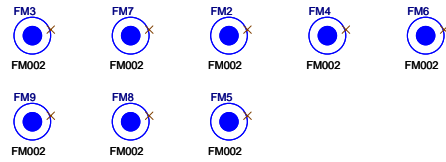
HEAT SINK

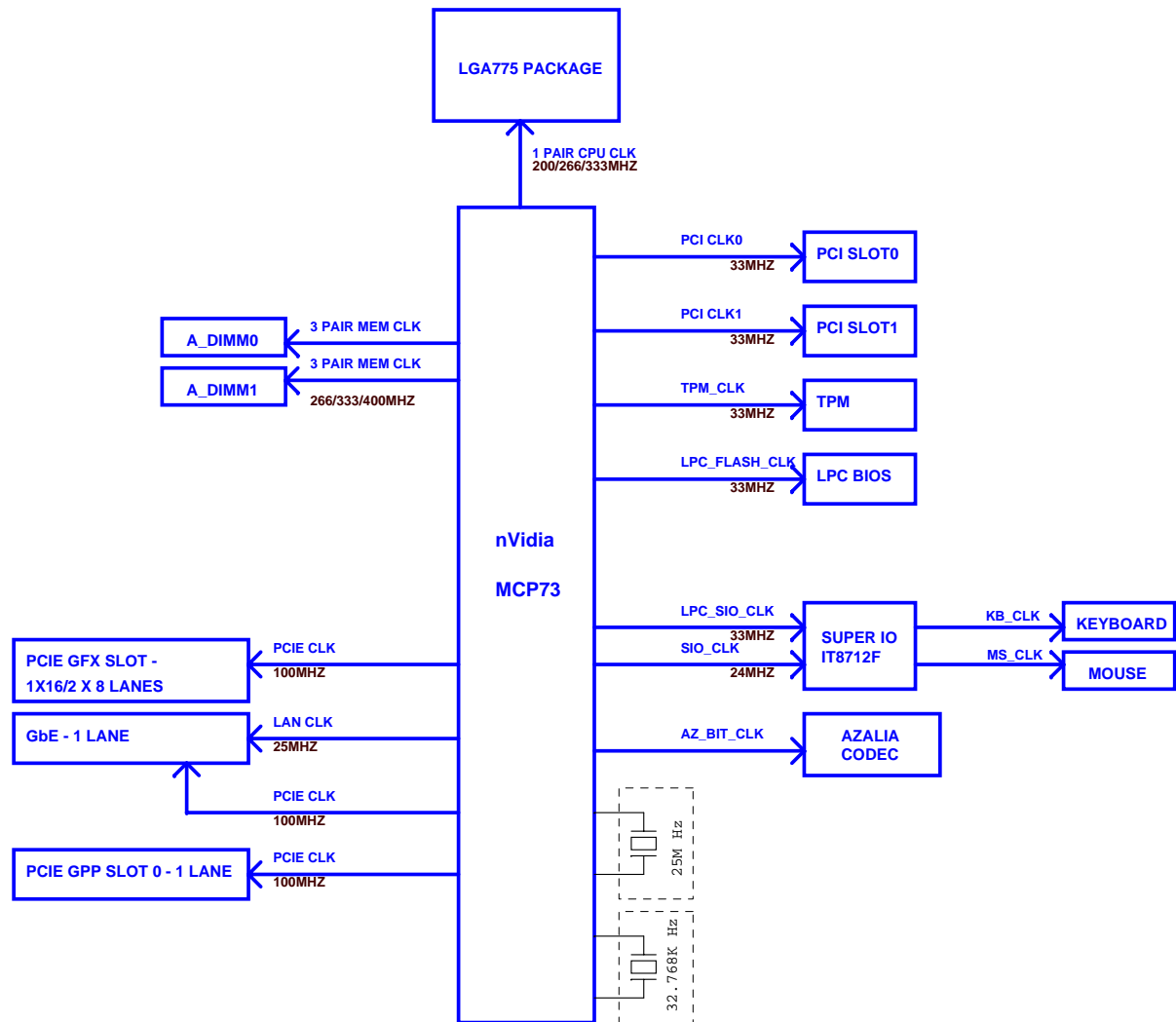


MANUAL PART



Optics Orientation Holes





ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

CPU PW
12V +/-5%

VRM 11 SW
REGULATOR

VTT 1.2V Linear
REGULATOR

NB_1P3V 1.3V
Linear Regulator

VCCP (S0, S1)

V_FSB_VTT (S0, S1)

NB_1P3V (S0, S1)

VCCCORE 0.84-1.85V 140A
VTT 1.2V 5A

+1.5V
SW REGULATOR

1.8V VCC_DDR
Linear Regulator

VCC_DDR (S0, S1, S3)

0.9V VTT_DDR
REGULATOR

VTT_DDR (S0, S1, S3)

DDRII DIMMX2
VDD MEM 7A
VTT_DDR 1.2A

1.3V STB LDO
REGULATOR

NB_1P3_SB (S0, S1, S3, S4, S5)

VCC3 (S0, S1)

5VAA LDO
REGULATOR

+5VR (S0, S1)

AUDIO CODEC
3.3V CORE 0.1A
5V ANALOG 0.1A

+3.3VSB REGULATOR
ACPI CONTROLLER

VCC3_SB (S0, S1, S3, S4, S5)

5VDIMM (S0, S1, S3, S4, S5)

ENTHENET
3.3V 0.1A (S3)
3.3V 0.5A (S0, S1)

nVidia MCP 73	
1.2V CPU VTT	800mA
V1P2_VDD_CORE 1.3V	5.7A
V1P2_PEX_DVDD 1.3V	450mA
V1P2_SATA_DVDD 1.3V	95mA
V1P2_PEX_AVDD 1.3V	1.3A
V1P2_SATA_AVDD 1.3V	380mA
V1P2_PLL_MEM_CPU 1.3V	60mA
V1P2_PEX0_PLLU 1.3V	170mA
V1P2_PEX1_PLL 1.3V	
V1P2_PLL_XREF_XS0 1.3V	45mA
V1P2_PLL_XREF_XS1 1.3V	
V1P2_SATA_PLL 1.3V	75mA
V1P2_PLL_SREF_SP 1.3V	10mA
V1P8_MEM_VDDP 1.8V	2.4A
V1P2_VDD_AUXC 1.3VSB	25mA
V3P3 3.3V	340mA
V3P3_DAC 3.3V	130mA
V3P3_HDMI_IO 3.3V	60mA
V3P3_PLL_COREPLL 3.3V	5mA
V3P3_PLL_XREF_XS0 3.3V	21mA
V3P3_PLL_XREF_XS1 3.3V	
V3P3_PLL 3.3V	30mA
V3P3_VPLL 3.3V	5mA
V3P3_PLL_SREF_SP 3.3V	15mA
V3P3_HDMI_PLL 3.3V	10mA
V3P3_DUAL 3.3VSB	50mA
V3P3_DUAL_USB 3.3VSB	75mA
V3P3_DUAL_RMG1 3.3VSB	35mA
V3P3_DUAL_PLL_MAC 3.3VSB	5mA

SUPER I/O
+3.3VDUAL (S3) 0.01A
+3.3V (S0, S1) 0.01A
+5V (S0, S1) 0.1A

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3VDual	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIE per	
3.3V	3.0A
12V	5.5A
3.3VDual	0.1A

USB X4 FR
VDD
5VDual
2.0A

USB X6 RL
VDD
5VDual
2.0A

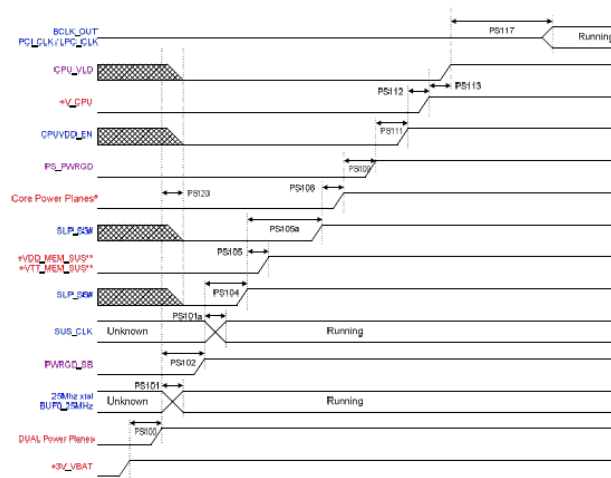
2XPS/2
5VDual
1.0A

VCC3_SB (S0, S1, S3, S4, S5)



MICRO-START INT'L CO.,LTD.

Power Deliver Chart		
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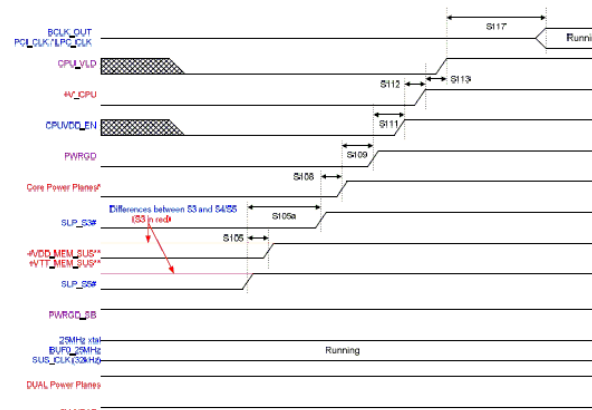


Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 G3-to-S0 Power-Up Sequence

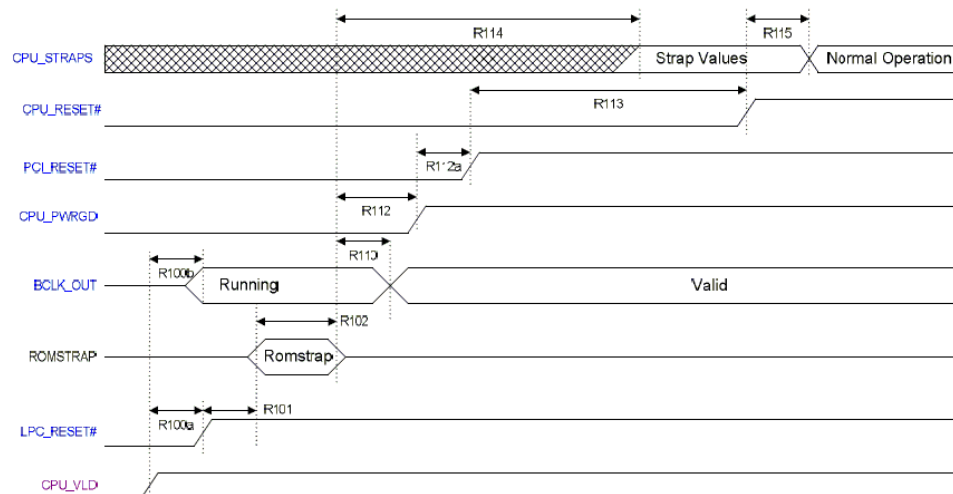


Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
- CPU Core Power Plane

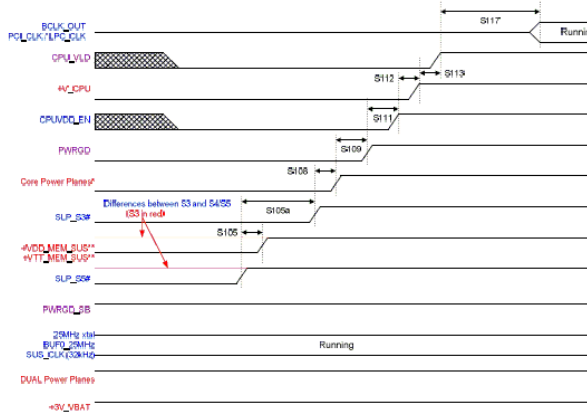
** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 S3/S4/S5 to S0 Power Resume Sequence



MCP73 output signals in Blue Motherboard generated signals in Purple

MCP73 Cold Reset Power-Up Sequence



Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
- CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 S3/S4/S5 to S0 Power Resume Sequence